Design-Analysis (Thermal and Mechanical) Integration Research for Electronic Packaging

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Abstract:

Simulating the characteristics of electronic packages like thermal resistance, thermomechanical stress distribution and electromagnetics is important to guide and verify their design. Since packages consist of densely packed components of varied materials and shapes, the simulation time for generating their finite element analysis (FEA) models can span from hours to days.

This paper overviews efforts to develop an automated tool aimed at one phase for CAD-CAE integration, that is FEA modeling. Automating idealized body decomposition and the use of SOAP have enabled a large-scale time reduction in FEA of packages while simultaneously providing the freedom to perform simulations across multiple platforms over the Internet. Additionally, proof-of-concept usage of STEP-based information models for chip packages (ISO 10303-210) holds promise for overcoming additional barriers in heterogeneous CAD-CAE transformations.

Nomenclature

ABB	analysis building block
API	application programming interface
APM	analyzable product model
EBGA	enhanced ball grid array
CBAM	context-based analysis model
COB	constrained object
FEA	finite element analysis
MRA	multi-representation architecture
SOAP	Simple Object Access Protocol
SMM	solution method model
STEP	Standard for Exchange of Product Model Data (ISO 10303)
XCP	*XaiTools ChipPackage*™

Introduction:

There is a pressing need to reduce the time and cost of product realization in the area of electronics packaging. Use of CAE tools to simulate package behavior is growing at an accelerating pace to reduce the need for physical measurements and trial production iterations. However, current tools do not fully address the needs of Concurrent Engineering especially for CAD-CAE integration in the thermal and mechanical areas.

Three-dimensional stacked and embedded packaging technologies for SIP (System in Package) abound with problems that were non-existent for two-dimensional applications. Figure 1 shows the FEA planning models for Plane and Stacked EBGA and Figure 2 shows their thermal resistance analysis results. As evident, the chip mounting area is reduced in the stacked case, but this also reduces thermal dissipation area. Hence, this can emerge as a thermal management problem even in low power device packaging applications.

These circumstances require an increasing use of CAE tools and reduction in the simulation time for producing more reliable packages. However, in the current state, there is a wide gap between CAD and CAE tools. Electrical CAD systems, which are primarily used for electronic package design, lack the interface for design data reusability by downstream CAE tools. Currently, an analyst must manually create an idealized geometric model in the preprocessor of the CAE tool. For the example shown in Figure 3, it can take an experienced analyst 6-12 hours to develop the decomposed model for the thermal resistance analysis of enhanced ball grid array (EBGA) packages.

We established collaborative design-analysis integration research between Shinko and Georgia Tech. to develop solutions for such problems.

Approach:

Figure 4 shows the basic concept of the Multi-Representation Architecture (MRA) for CAD-CAE interoperability and associated ubiquitization methodology [1,2]. The MRA has been developed to realize the transformations from design to analysis through four stepping stone information representations. On the right side is solution method model (SMM), marked with ? , which represents an analysis model in relatively low level and solution method specific form. An SMM combines solution tool access and results retrieval. Analysis building blocks (ABBs), marked with ? , represent engineering analysis concepts in a manner that is largely independent of product application and solution method. ABBs obtain results by generating SMMs through transformations, $_{ABB}\Psi_{SMM}$, that are based on solution method considerations.

Analyzable Product Model (APMs), marked with ? , represent detailed and design-oriented product information. An APM is considered as the master description of a product, which supplies high-level information and enables usage by potentially many analysis applications. Context-based analysis models (CBAMs), marked with ? , contain linkages that represent design-analysis associativity between APMs and ABBs, $_{APM}\Phi_{ABB}$. Such linkages indicate the usage of idealizations for particular analysis applications. From the MRA viewpoint, providing solutions to the design-analysis integration problem involves defining the four representations (SMMs, ABBs, APMs, and CBAMs) and two inter-representation mappings ($_{ABB}\Psi_{SMM}$, $_{APM}\Phi_{ABB}$). In this paper we primarily focus on ABB models for solid mechanics and thermal systems that utilize FEA-based SMMs.

Figure 5 shows a roadmap for FEA-based design-analysis integration broken down into several levels of abstraction and modularity. The heterogeneous transformation, which is the overarching objective, is indicated as Level 0. Level 1 depicts the analysis-specific idealizations of the original CAD model. The next lower level, Level 2, shows the MRA approach. In Level 3, the inter-representation mapping $_{ABB}\Psi_{SMM}$ has been further broken down into two mappings $_{ABB}\Psi_{RMM}$ and $_{RMM}\Psi_{SMM}$. As a result, the intermediate model, Ready-to-Mesh Model (RMM) is introduced.

A detailed description of Level 3 is shown in Figure 6. Generally, an analytical model is created by assembling idealized bodies together using idealized interconnections. These idealized bodies must be decomposed to RMMs to enable finite element node matching. The main challenge is to develop an automated decomposition algorithm that satisfies node matching and is generic to adapt to variable topologies and diverse vendor meshing capabilities.

Chip package thermal analysis models typically consist of a number of idealized bodies (e.g., 20-30 bodies) of different materials (e.g., 10 or so). These bodies are tightly packed together. Thus the meshing of one body can strongly impact the meshing of bodies that are not directly adjacent to it. Targeting those challenges, a decomposition algorithm (a.k.a. chopping[1]) has been developed[2] to manipulate model geometry to ensure automatic mesh node matching even for these tightly coupled body cases. (Figure 7) [3].

Figure 8 illustrates an example ABB assembly representation. The assembly model consists of two idealized bodies and two connectivity constraints that describe the idealized interconnections between these two bodies, denoted by C1 and C2. Loading constraint L1 represents an active pressure applied onto one of the bodies. The rigid support along the right hand face is denoted by the support constraint S1. The ABB assembly model, in the decomposed state, is illustrated in Figure 9. Bodies are decomposed and constraints are also decomposed while maintaining the constraint relations hierarchically.

Usage Overview:

Figure 10 is the panorama context of this work, which shows design tools (on the left) with general-purpose CAE tools (on the right). A web-based design tool has been developed in this work.

CAD systems typically do not support adequate interfaces to capture and access the information needed by chip package simulation models. Thus, we capture design information in a custom information template structure, which is described in STEP Express (ISO 10303-11). Then the data is taken into *XaiTools ChipPackage*™ (XCP) the model is automatically decomposed, and the simulation is executed on the analysis solvers.

A package design model is first created in this process that includes geometric features and material models, via the web-based user interface, as shown in Figure 11. Design information

[1] Tom Mack, MSC Software.

[2] PhD thesis underway in this area (by Sai Zeng).

transformed to the custom STEP-based description is then taken into XCP. XCP is developed as an end-user-oriented STEP-Book application (a technology initiated by LKSoft, GmbH). Figure 12 shows an example of the EBGA thermal analysis model view. The model information tree, displayed on the left side and the information regarding the specific leaves, as shown on the right side, enables the user to easily retrieve the needed information (e.g. chip size, young's modules, etc.).

XCP also provides three-dimensional geometric model viewer capabilities based on standard STEP capabilities (ISO 10303-514). Undecomposed and decomposed ABB assembly views are shown in Figure 13, 14. Operations such as pan, zoom and rotate can be performed in the 3D viewer, for a detailed view of the geometric model, using simple mouse operations.

The step-by-step operation procedure for thermal analysis in XCP is performed in the order shown in Figure 15 (or a single button push is possible to run everything all at once). "*Solve ABB*" solves for the geometrical relations of ABB. Then, "*Chop ABB*" decomposes the ABB. An SMM for a preprocessor (PATRAN)-dependent model, is created in the next step: "*Setup FEA SMM*". "*Solve FEA*" executes the analysis solver (ABAQUS) on the said SMM.

After the analysis job has been done, "*Update FEA SMM*" loads the results back into XCP and transforms them from generic FEA data into chip package-specific knowledge (e.g., thermal resistance values). XCP displays the computed numerical and graphical results. Figure 16 is an example for EBGA thermal resistance results that displays temperature values and distribution contour. In the stress analysis case, deformation, stress distribution contours, and maximum and minimum stresses on each block are displayed.

XCP uses an Internet standard called SOAP[3] (Simple object access Protocol), which enables the access to the solver server from a remote client across the Web. Data exchange and remote procedure calls are done between the client and server. Thereby, an efficient system operation is achieved by distributing low memory intensive operations like XCP usage on the client side and high memory intensive tasks like decomposition module execution and FEA solution on the server side (Figure 17). These operations have successfully been tested between Shinko (Nagano, Japan) and Georgia Tech (Atlanta, GA, USA).

Ideally standards-based CAD models could be leveraged directly from the CAD tools. A trial data translation example from CAD to STEP-Book AP210 is shown in Figure 18. This test design is an assembly model that consists of a simplified chip, the substrate and solder balls. This test design was captured in the EAGLE[4] electrical CAD system (CadSoft Computer GmbH) since a STEP AP210 translator was already available for it (by LKSoftWare, GmbH). The translated information model for this example is shown in Figure 19. The detailed information about the selected solder ball instance (left side figure) is displayed in the table (on the right side).

STEP AP210 interfaces for other ECAD tools like Zuken and Mentor Graphics are now at the alpha level of development at LKSoft[5]. Hence, in the future, tools like XCP will be able to more easily support analysis simulations for electronic packages designed across varied CAD systems that have an AP210 interface or a converter.

Results:

Based on industrial usage and testing, Table 1 summarizes the analyst efforts required for model creation activities for various analysis models. In the case of thermal analysis, it takes 6-8 hours to create the thermal analysis model using the traditional method. On the other hand with the use of the new concurrent engineering tool, XCP, the modeling time has reduced from 8 hours to 39 minutes. Reduction in the modeling time is of the same order even in the case of stress analysis. Although the decomposition time increases for complex models, the manual effort is still greatly reduced, and we expect further improvements in decomposition algorithm efficiency.

XCP combined with this new decomposition algorithm has the capability to add analysis templates for new types of packages without complex programming. Furthermore, this tool has paved the way for simulation usage by people who do not have detailed knowledge about analysis simulations (e.g. design and sales engineers) by the application of interoperability and Internet technologies.

[3] SOAP is an Internet protocol based on XML, which performs a remote procedure call and data exchange in order to achieve automated web services. See www.w3.org for further information.

[4] See http://www.cadsoft.de for more information.

[5] See www.lksoft.com for examples and the latest status.

Conclusion:

This paper overviews collaborative efforts in the area of design-analysis integration technology between Shinko and Georgia Tech. To enable highly automated analysis modules, engineering information technology has been applied to semiconductor chip packaging.

This work has achieved the following benefits:

1) Decreased FEA model creation time (factor of 10:1 or more, from days/hours to minutes)
2) Enabled more analysis iterations to study wider design variations, leading to an improved design.
3) Provided new usage possibilities via a web-based distributed architecture (e.g., increased potential user audience such as sales engineers around the world for quick customer feedback). This can also increase solution tool usage efficiency (more usage per license). It is however, a single component in an enhanced collaborative product realization environment and there is a large potential for further developments in this direction.
4) Enabled the easy addition of new analysis templates without complex programming. (made possible by a new decomposition algorithm).
5) Increased the span of the XCP design input interfaces to a wide range of CAD systems (which can support the STEP neutral information modeling format).

References:

[1] Peak, R. S.; Scholand, A. J.; Tamburini D. R.; Fulton, R. E. (1999) Towards the Ubiquitization of Engineering Analysis to Support Product Design. Invited Paper for Special Issue: Advanced Product Data Management Supporting Product Life-Cycle Activities, *Intl. J. Computer Applications in Technology*, Vol. 12, No. 1, 1-15.

[2] Peak, R. S. (1999) X-Analysis Integration / Multi-Representation Architecture (XAI/MRA) Overviews. http://eislab.gatech.edu/

[3] Koo, D. (2000). A Product Data-Driven Methodology for Automating Variable Topology Multi-Body Finite Element Analysis. Masters Thesis, Mechanical Engineering. Atlanta, Georgia Institute of Technology.

[4] XFW (2001). XaiTools Frame Work™ *http://eislab.gatech.edu/tools/XaiTools/*

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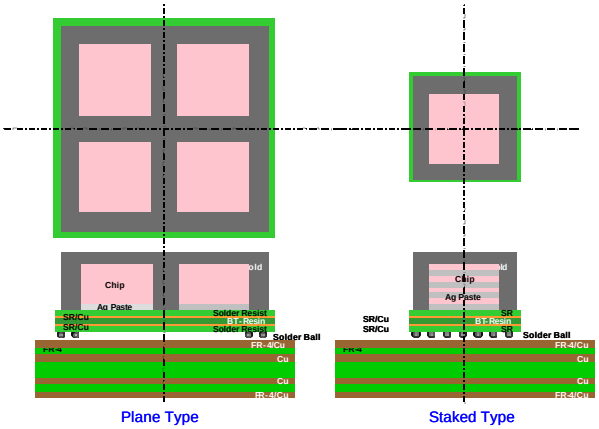

Figure 1. FEM Simulation Models for Stacked and Plane BGA

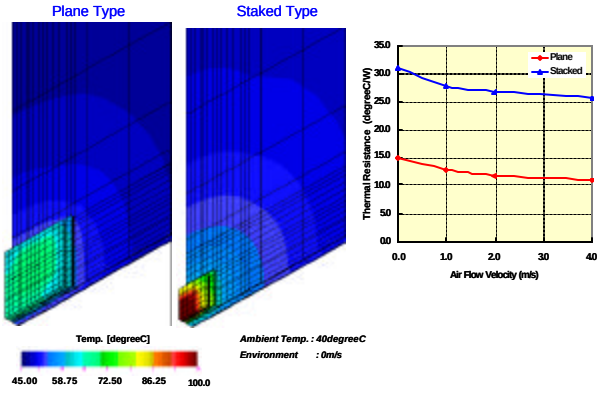

Figure 2. Thermal Simulation Results

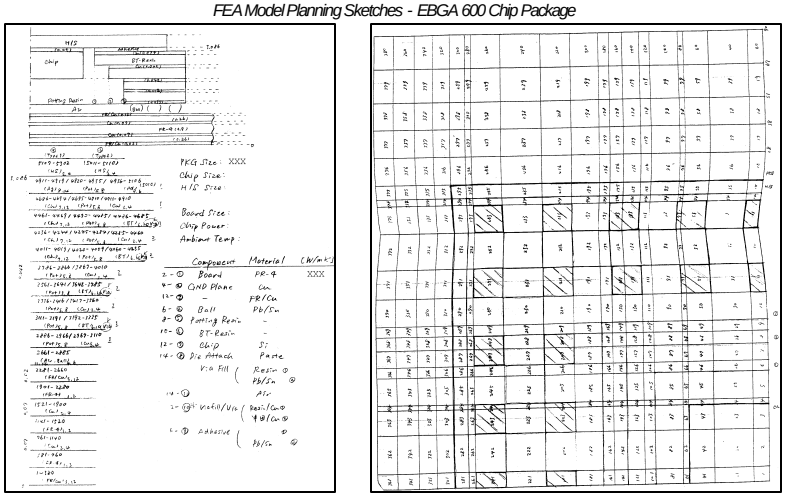

Figure 3. Traditional creation of variable topology multi-body VTMB FEM models

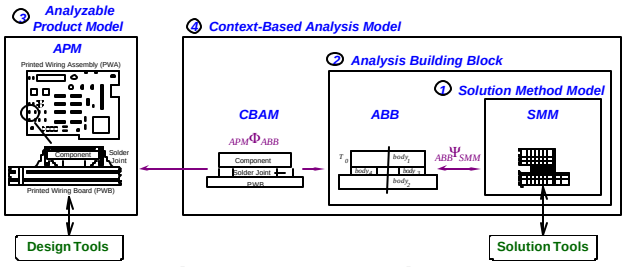

Figure 4. Multi-Representation Architecture (MRA)

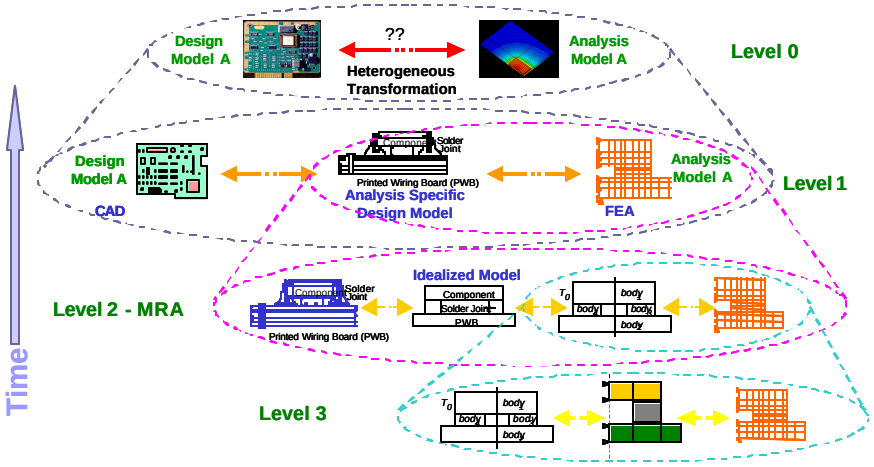

Figure 5. Advanced FEA Modeling Roadmap

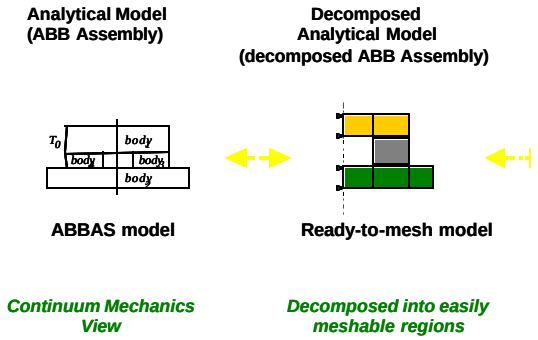

Figure 6. Main Stages at Level 3
for Generating Complex FEA Models

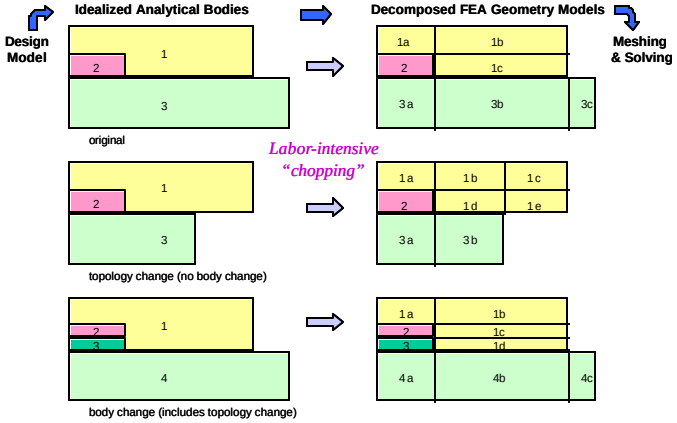

Figure 7. Variable Topology Multi-Body (VTMB)
FEA Meshing Challenges

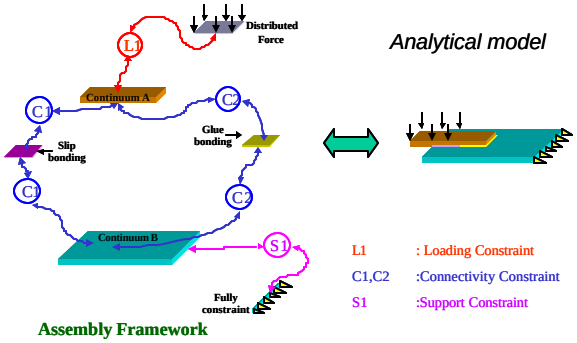

Figure 8. ABB Assemb ly Representation
(Original State)

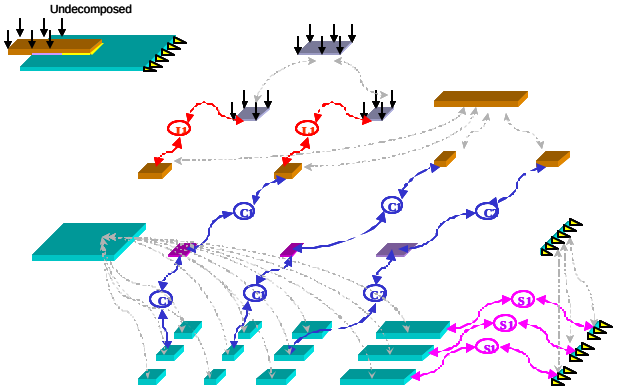

Figure 9. ABB Assembly Representation
(Decomposed state)

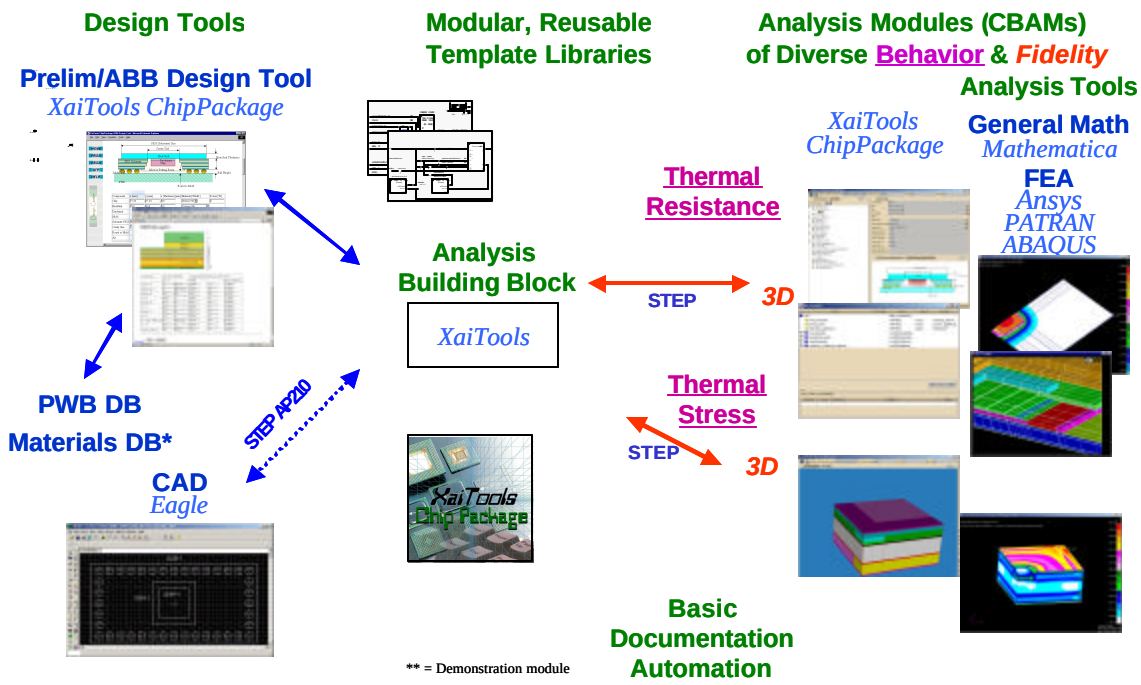

Figure 10. Flexible High Diversity Design-Analysis Integration

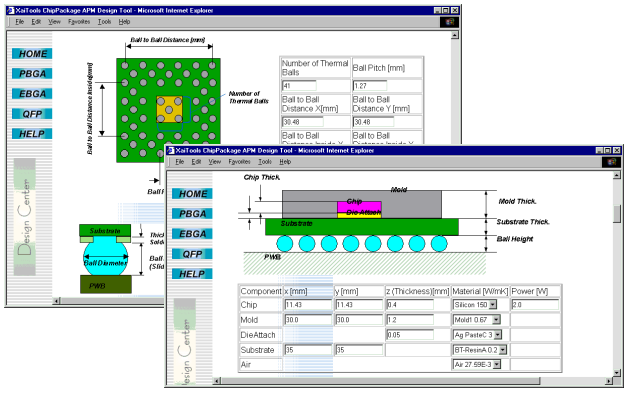

Figure 11. Web-based chip package preliminary design tool

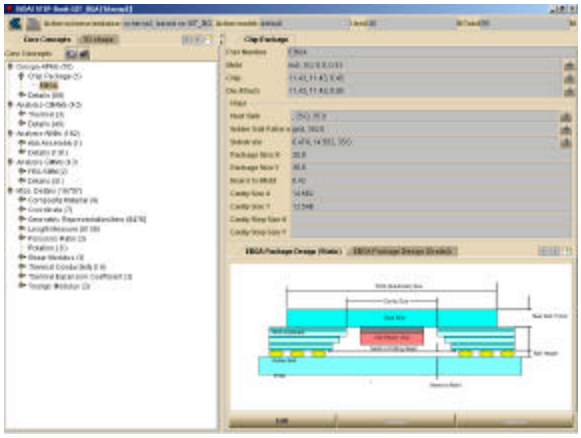

Figure 12. *XCP* for BGA Thermal Analysis Templates

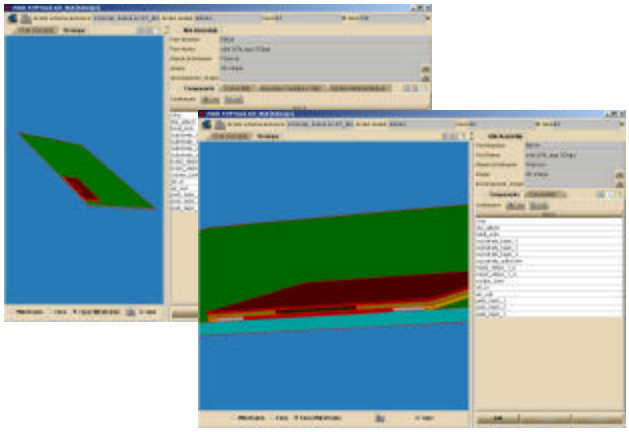

Figure 13. 3D view of the ABB assembly (undecomposed bodies –before chopping)

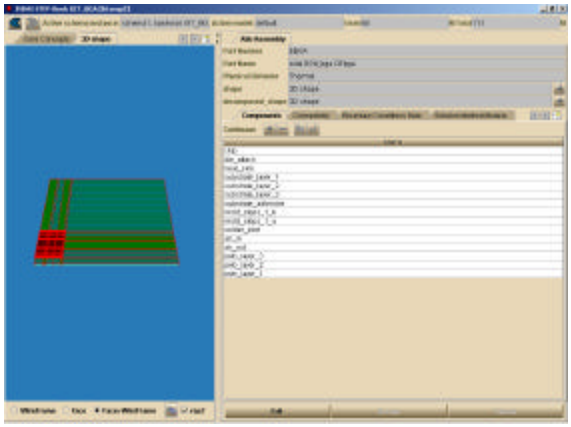

Figure 14. 3D view of the ABB assembly (decomposed bodies - after chopping)

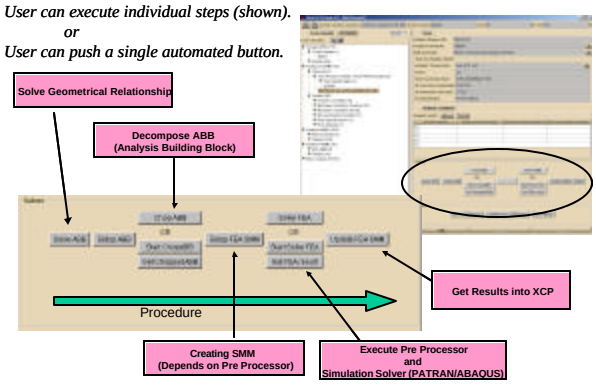

Figure 15. Analysis Procedure

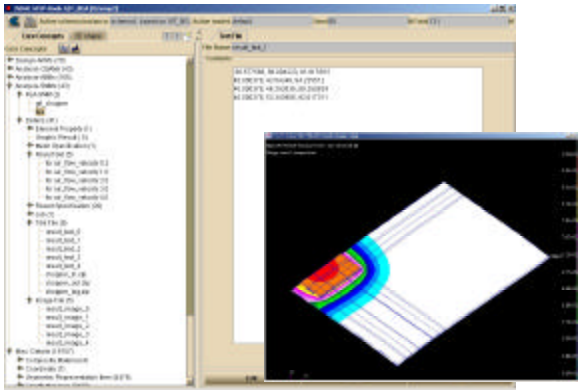

Figure 16. Viewing detailed results in SMM context

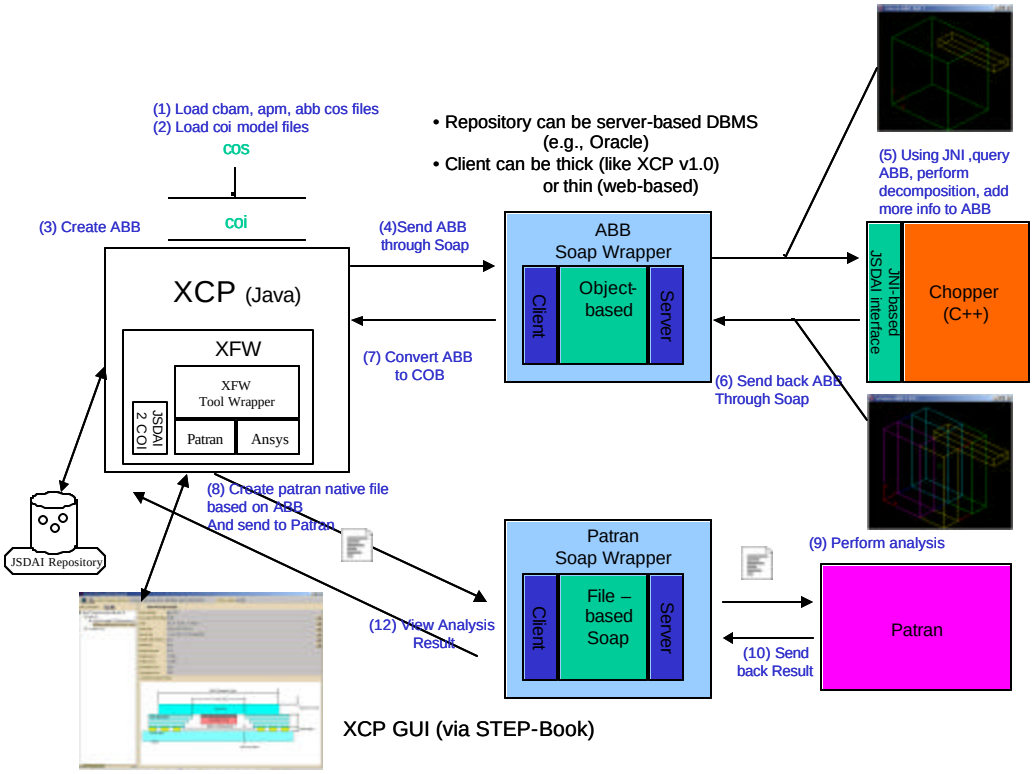

Figure 17. XCP Architecture (Developer's View)

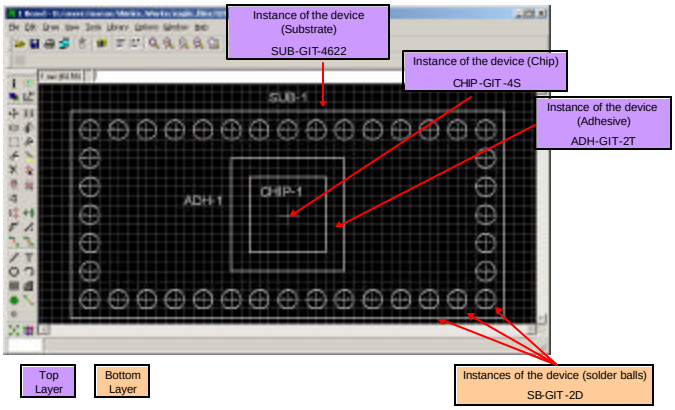

Figure 18. Chip package test case (in the EAGLE ECAD tool)

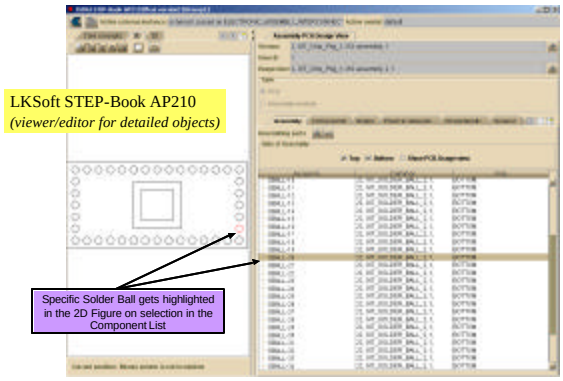

Figure 19. Chip package test case (in the STEP-Book AP210 tool after translation into the ISO 10303-210 neutral model format)

Table1. FEM Modeling Time Reduction

Analysis Model Creation Activity	With Traditional Practice	With Decomposition Algorithm
Thermal Model EBGA352	6-8 hours	8 minutes
Thermal Model EBGA600	6-8 hours	39 minutes
Stress Model Case1	2 hours	5 minutes
Stress Model Case2	1 hours	2 minutes