



# SysML in Factory Modeling

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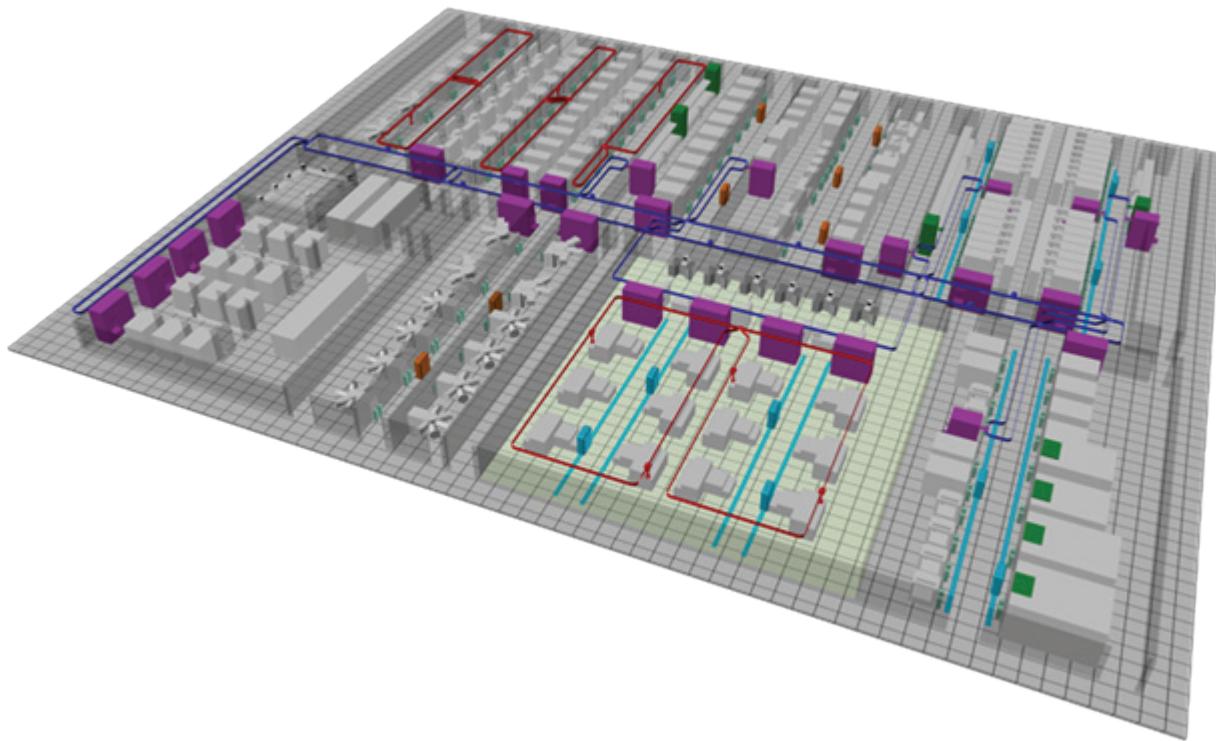
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*Presentation to*  
OMG Systems Engineering  
Domain-Specific Interest Group (SE DSIG)

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# Modern Wafer Fab



- ~  $10^3$  process tools
- ~  $10^3$  lots in process
- ~  $10^3$  steps per lot
- ~ 30 layers per wafer
- ~ 60 days cycle time

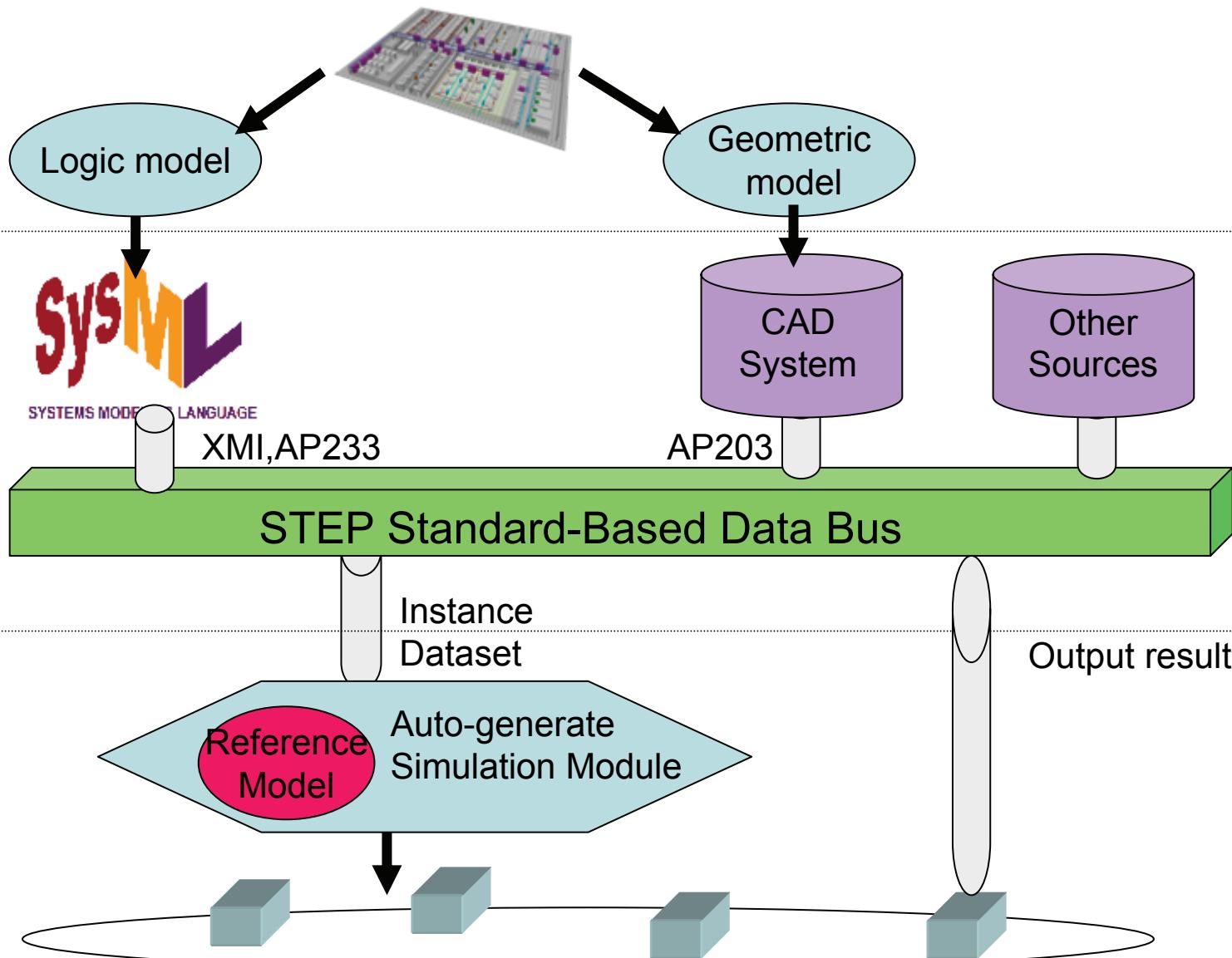
The only way to accurately predict manufacturing performance is to use a high-fidelity discrete event simulation model. These models are hand-build without engineering tools for capturing requirements or technical data describing the fab.

# Data Capture for Simulation

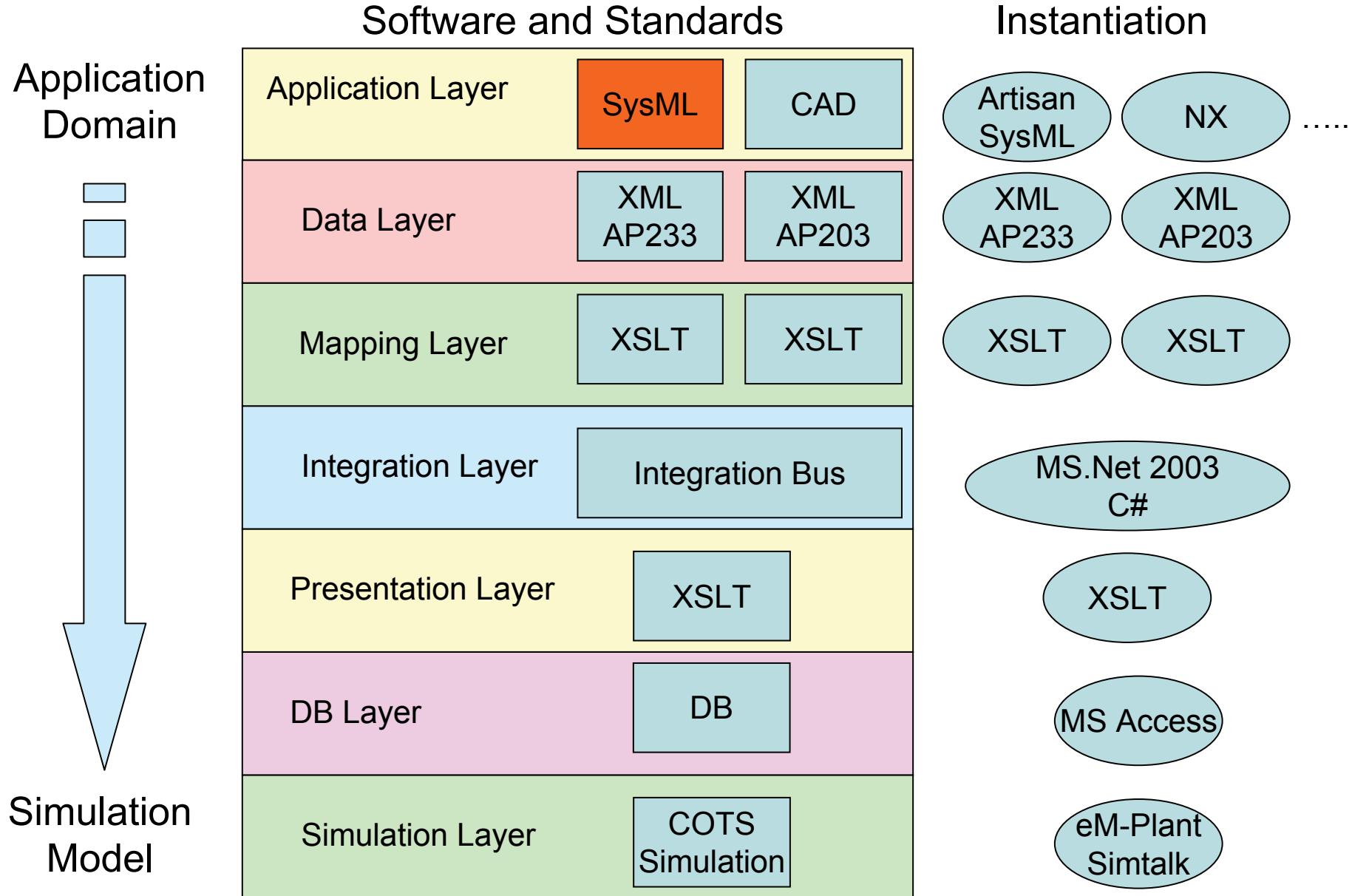
Factory Aspect	Tool	SysML Elements
<ul style="list-style-type: none"><li>• Resource models<ul style="list-style-type: none"><li>– Tools</li><li>– Storage</li><li>– Transportation</li><li>– People</li><li>– Layout</li></ul></li></ul>	<ul style="list-style-type: none"><li>SysML</li><li>SysML</li><li>SysML</li><li>SysML</li><li>CAD</li></ul>	<ul style="list-style-type: none"><li>Block / Class</li><li>Block / Class</li><li>Block / Class</li><li>Class / State</li></ul>
<ul style="list-style-type: none"><li>• Product model<ul style="list-style-type: none"><li>– Process plans</li></ul></li></ul>	SysML	Sequence / Activity
<ul style="list-style-type: none"><li>• Behavioral model<ul style="list-style-type: none"><li>– Orders</li><li>– Schedules/Sequence</li></ul></li></ul>	<ul style="list-style-type: none"><li>Excel</li><li>SysML</li></ul>	Sequence / Activity

# Scope Overview

Shop Floor System



# Proposed Architecture



# Progress To Date

- SysML data capture and standards-based data schema
- Simulation model generation from standard data schema
- Pending: CAD-based geometry capture and standard data schema