Summary

Based on the observation that there are limited components used to fabricate a product, and limited types of interconnections in a component assembly, a novel approach, so called Modularized & Parametric Finite Element Modeling methodology, has been developed to provide a promising capability for analyzing an entire featured electronic product in much less time without loss of accuracy. Several disciplinary techniques and algorithms have been investigated, and then integrated into a conventional Finite Element Method (FEM) code

Electrical components are classified into a limited number of categories by taxonomic technique. These components are further decomposed into Modularized Geometry Primitives (MGPs). MGPs are used as the most basic building blocks for a product model assembly. Each MGP is created by using a parametric modeling approach. The parametric modeling approach is to create or define a model template by parameters and its forming rules, instead of a specific model. The template is used to generate an actual analysis model by populating data into the parameters of a template. A template serves as a master model mock-up, and is applied for one-to-many modeling activities. A graph tree so called Constructive Module Assembly Tree (CMAT), is developed to represent the relations of MGPs and the product assembly. A few graph algorithms are developed to assemble a FE model for the product by using CMAT. A divide-and-conquer algorithm is developed to model a multi-layer PWB substrate with copper traces. This algorithm partitions the board into small sections, such that each section can be individually modeled and assembled back to represent the original board. Two case studies have been performed to test the capability and flexibility of the developed methodology. From the study results, it has been concluded that the developed methodology is a very cost-effective and vital tool for thermomechanical design of an electronic product.

Given the challenge to improve product quality and reliability, while decreasing product cost and “time-to-market”, an approach, identifying the key characteristics that can contribute to thermal and/or mechanical failure, has been pursued.

Part I

Literature Survey

Advanced electronic Packaging Technology

Literature reviews of current electronic packaging technology are presented as the first part of this research study. It shows a snapshot of the electronic packaging technology taken in the electronic industry during the recent critical period of ongoing evolution from IMT to SMT, and beyond. It is believed that the understanding of various packaging technologies is very beneficial to develop good thermomechanical models. Chapter 1 briefly introduces the trend of electronic products and the motivations of this research study. Chapter 2 presents the general definitions of the terminology in electronic packaging technology. Chapter 3 reviews the design processes and considerations during an electronic product development. Chapter 4 overviews the current state of thermomechanical design analysis and modeling activities.

Chapter 1

Introduction

Dramatic changes are underway in computer, telecommunication, automotive, and consumer electronic industries[68]. In computers, advanced semiconductor technology and architecture have ignited a significant down sizing of an "enterprise computing" environment, and a rapid emergence of microprocessors for high-end applications. There is a similar trend in telecommunications, where high performance, multifunctional, portable units are becoming popular, such as multimedia product, cellular/ wireless equipment, advanced HDTV, and visual communication devices. In addition, more sophisticated and functional electronic devices have been brought to home making our everyday-life more pleasant. Major change has also occurred in automotive industry, as more active electronic devices are supporting the Intelligent Vehicle Highway System (IVHS)[68]. The major trend of these changes are to make products more powerful, functional, reliable, and personable, while at the same time greatly reducing the cost, size, and weight.

These significant improvements are primarily due to the advance of electronic packaging technology. Electronic packaging technology is the art of placing functions in a limited room that is space efficient, cost effective, performance attractive [59]. With the large integration of electronic circuit, heat concentration and structural failure have come to be vital reliability issues for electronic packaging designs and analyses[32]. Although an increasing number of mechanical engineers have been involved in the

research and development of electronic packaging, mechanical and thermal phenomena are among the least understood and most complex of the many phenomena encountered in an electronic packaging system[6,19,49,58].

Today, mechanical design, especially thermomechanical behavior design, is typically considered only at the final stage of the design process. In the interest of shorter turnaround time and the need for a single-pass manufacturing cycle, mechanical design has to be made up front with other design decisions. This requires mechanical computer aided design (MCAD) tools to be integrated into the electrical computer aided design(ECAD) system[12]. The integration of E/MCAD system may provide a design decision, based on an optimum balance among the many requirements and constraints. Concurrent mechanical design, with electrical, may recognize and eliminate the thermomechanical failure mode prior to final product design, and so generate a "failure-free" product which is "correct by design"[4].

However, most of the available MCAD systems are used primarily for drafting, layout and parts lists, but only marginally affect the realm of an engineering analysis. To respond to the growing needs of mechanical modeling and the simulation in electronic design process, a new approach, Modularized & Parametric Modeling Methodology, has been developed in this research.

This thesis addressed what shall be done to further develop and unitize the mechanical modeling tools, as warranted by the ever-increasing demand of thermomechanical analysis and simulation in electronic product design. Several disciplinary techniques and algorithms have been investigated, and then integrated into a conventional Finite Element Method (FEM) code. Given the challenge to improve product quality and reliability, while decreasing product cost and "time-to-market", an approach, identifying the key characteristics that can contribute to thermal and/or mechanical failure, has been pursued.

Chapter 2

Overview of Advanced Electronic Packaging

Since the invention of Integrated Circuit (IC), the density and performance of electronic devices have been increasing at an exponential rate. The improvement of circuit design, process modeling, and layout techniques have led to a dramatic change in size, speed, and cost of electronic systems. One of major technology switch is from Insertion Mount Technology (IMT) to Surface Mount Technology (SMT). In addition, the switch from Wire Bond (WB) to Tap Automated Bond (TAB) and/or Flip-Chip, from packaged chips to unpackaged chips, and from Single Chip Module (SCM) to MultiChip Module (MCM), will be inevitable in the near future.

This chapter shows a snapshot of the electronic packaging technology taken in electronic industry during recent critical period of ongoing evolution from IMT to SMT, and beyond. The first section presents the general definitions of the terminology of electronic packaging. Section 2.2 includes major techniques used to bond bare chips (Die) to substrates. Section 2.3 shows classification of packaging technology. Section 2.4 describes some issues that designers have to overcome to create reliable, high performance, and low lost products.

2.1 General Definition of Electronic Packaging

The bottleneck of these modern electronic circuits, devices, and assembly is elec-

tronic packaging technology. Electronic packaging can be defined as a structure, which contains many circuits. It has functions of signal interconnection, power distribution, heat dissipation, and circuit protection. Every time an IC is used in any electronic product, it must be packaged. A selected packaging technology is a trade-off among performance, cost, reliability, and manufacturability.

As a general rule, several levels of packaging are often needed in an electronic assembly [59]. They are often referred to as a packaging hierarchy. Silicon integrated circuit chip itself is called as zero-level (chip level). The chip capsulate, which houses the chip as a pluggable or mountable component, constitutes the first level of packaging. Connections between chip and package is refereed to as chip-level interconnection. They are commonly performed as wire bond, TAB, or Controlled Collapsed Chip Connection (C-4). The first-level packaging structure must not only provide the power and signal transmission, but must also structurally support the chip and establish a path for effective heat removal. Chip-to-chip interconnection on a substrate is deemed the second-level of packaging hierarchy. Substrates typically are printed circuit cards or ceramic modules. In the third level of packaging hierarchy, the cards are further connected to a third level board, which is used for card-to-card interconnection. The board has multi-layered structure and contains connector to accept cards. A box or rack, which includes the complete system, houses the fourth level of packaging hierarchy.

Packaging technology plays a critical role in determining system speed and performance. The efficiency of a product in performance and size can be referred to Silicon Efficiency (SE) [66]. It is the ratio of the total area occupied by silicon to the total board (substrate) area. The SE of a typical Printed Wiring Board (PWB) with several individually packaged VLSI-chips is around 5%. The area saving can be an order of magnitude or more, if all the chips are directly mounted onto the board. High silicon efficiency will normally result in superior electric performance, better reliability and lower cost.

2.2 Chip Bonding Technology

The electrical connections between a bare chip (die) and a package (or substrate) is refereed to chip bonding technology (chip-level interconnection technology). The technique used to bond dies to substrates or packages affects the maximum achievable silicon efficiency. It also has a great impact on the performances of electrical, mechanical, and thermal properties of the packages. There are four popular bonding technologies currently in practice: Wire Bonding (WB), Tape Automated Bonding (TAB), Flip-Chip, and Overlay. It is important to note that no chip-level package can accommodate all the required chips and functions. A second-level package interconnecting chip-level is generally required. The technologies used for this level of interconnections, so called as package-to-substrate technology, can be found in references [59 - 64].

2.2.1 Wiring Bonding

Wire bonding is the traditional bonding technique used in microelectronics industry. Bell Laboratory first introduced this technique in 1957. It was called thermocompression Bonding. Now, it is still the most common chip-connection technology used for Single Chip Package (SCP).

In this technique, a chip is first attached to a substrate, using a special thermally conductive adhesive, with I/O pad side (active side) facing up. The wires are then bonded, one at a time, to the chip and substrate. Three different bonding process are available: thermocompression (TC) bonding, ultrasonic (UC) bonding, and thermosonic (TS) bonding. For most applications, the bonding wires are about 25 to 38 micron in diameters. The materials used for bonding wires have to be customized to a range of mechanical properties for a deserved break strength and elongation. Common bonding materials are Aluminum wire, Aluminum-Magnesium wire, and gold bonding wire. The wire diameter, and the pad pitches of chip and substrate are two important design

factors. The shape and length of bonded wire should be optimized for its reliability. Most reliability failures are due to manufacturing defects. With the improvement of manufacturing process, reliability failures have been considerably decreased. Reworking a defective chip is relatively complex. Each wire has to be removed, and die has to be debonded. Then, a new chip is placed, and followed by a new wire bonding process.

Dramatic advances have been made in wire bond rates by automatic bonding machine, and resultant cost reductions are significant. The bonding operations can be performed in less than 0.2 second per bonding cycle. Fully automatic chip mounters for die bonding have also been developed. A number of wire bonding tools are available in the market for different applications. Because of the mature of wire bonding technique, it does not require much equipment cost and R&D effects. However, since the connections are formed one at a time, this technique is not efficient for chips with very high pin counts. WB technique can not handle area array interconnection, because it can only handle a chip with I/O pads located on the perimeter of the chip. The parasitics of the bonding wires may introduce signal degradation in a high-speed application. Thus, WB is cost effective for applications do not require very high density or performance.

2.2.2 Tape Automated Bonding

In tape automated bonding (TAB), a bare IC is first bonded to a carrier, which is a long roll of flexible tape similar to a photographic film. A series of identical, fine pitch copper wire patterns are deposited onto the film tape. The function of TAB is to terminate an active chip to a substrate. This technique was initiated in the 1960s by General Electric Co. (GE), and has been further developed by many major semiconductor manufactures.

The TAB process involves bonding silicon chips to the patterned metal on a film tape. Once the chips are bonded to the tape by inner-lead bonding (ILB), the individual chip carriers can be cut out off the tape, and pads on the TAB carrier can be attached to

the substrate by outer-lead bonding (OLB). The tapes used for TAB can be prepared in many forms, involving different material, width, plate surface, and geometry. Basic tape variations are one-, two-, and three-layer tapes. All three types of the tapes are normally designed to provide the optimal ILB or OLB operations, as well as the required lead life and corrosion resistance.

The TAB process is easy for automation, and fast for volume production. The abilities of pretesting and burning chips, prior to the final assembly, is the major advantages of TAB. These abilities greatly increase the confidence of good bare dies, and increase module yield. However, the silicon efficiency is not as high as other techniques, due to the occupied TAB lead space. The major problem with TAB is the lack of I/O standards of chips. Every chip has potentially different I/O position and I/O quantities. This makes the standardization of TAB pattern practically impossible.

2.2.3 Flip-Chip

Flip-chip technology, is originally used at IBM in 1960s. It has numerous acronyms. In industry, it has been called as Controlled Collapse Chip Connection (C4), Controlled Collapse Bonding (CCB), or Flip-Chip Joint. In this technology, solder bumps are added onto I/O terminal pads of a chip, which is conventionally processed in wafer form, by plating, or evaporation. Bare chips are placed face down onto a substrate, so that the bumps align with the contact pads on the substrate surface. The substrate are commonly made from silicon or ceramic with CTE from 2 ppm to 7 ppm. The assembly is then reflowed to simultaneously form all the contacts.

Flip-chip technology, in near future, will play a major role in electronics industry. It has shown some significant advantages. The silicon efficiency is very high. Zero area is needed for chip interconnection, unlike WB or TAB. It is especially advantageous in high speed applications, due to the low interconnect inductance. The

assembly process exhibits a “self-alignment” characteristic, due to the surface tension of solder. The same process can be used for chips with area array of I/O pads. Repairability is also possible with specialized tools.

However, this technology currently has a few drawbacks that limit its general use. Large volume of pretested and bumped chips are not available. Due to the mismatch of coefficient of thermal expansion (CTE) between the chip and substrate, the reliability of large flip-chips on the substrate is still questionable. Thermal transfer from chips to substrate is also limited.

Until recently, a conventional printed wiring board (PWB) is used as flip-chip substrate. It has been called as Flip chip on board (FCOB) technology, direct chip attach (DCA), or flip chip attach (FCA). It has received increasing attention as a way to improve package density and electrical performance at a low cost. Compared to the similar but more matured C4 technology that requires reflow temperature up to 320 ^{o}C for lead-rich tin/lead (3/97) solder bumps, the FCOB process involves a lower reflow temperature by using eutectic solder (63/37 tin/lead alloy) to join the chip solder bumps to the substrate. For this reason, the FCOB process can be used for the traditional low cost organic, epoxy-based printed wiring board (PWB) assembly process. Although the FCOB technology provides definite advantages over the C4 and traditional SMT packaged component assemblies, reliability concerns have been raised due to higher coefficient of thermal expansion (CTE) mismatch between the silicon die (around 3-4 ppm/C) and the organic substrate (16-26 ppm/C).

2.2.4 Overlay

A relatively new approach to interconnect chips is the overlay interconnect technology. General Electric, teamed with Texas Instruments, has developed a High Density Interconnect (HDI) chip-first process for the interconnection of Multichip Module (MCM) in early 1990s. GE/TI HDI overlay MCM technology has being commercialized

through with Teas Instruments. Several designs constructed with overlay interconnect demonstrate the highest frequency operation and thermal performance of MCMs to date. System design will be described with 400 mHz, and has great clock operation and dissipating 50 watts.

Unlike most other chip bonding technologies, which have dies placed on the top of an interconnect structure, the overlay process builds the interconnect over the top of bare dies. The substrate is not the finished interconnect structure as in other technologies, but rather a heat sink and supporting structure for the chips and interconnect. The chips are placed into one or more cavity recessed whose depths match the chip thickness. A thin film polyimide sheet is laminated over the die and the exposed substrate surface. Vias are drilled through the dielectric to the die bonding pads, and to the substrate I/O pads. Metal and photo resist are applied, exposed, and removed with standard semiconductor and PWB process. The interconnection pattern is applied to the photo resist using the direct laser-write process. The overlay process is repeated to complete the interconnect. Since chips can be placed with very little separation, the silicon efficiency can be reached as much as 90 percent.

The GE/TI HDI structure, with its electrical path upward and its thermal path downward, is optimized for high frequency, high power circuits. Because the overlay interconnect provides direct connection between ICs and controllable impedance strip line and microstrip structures, it eliminates the electrical losses due to long length PWB interconnect, and the low pass filtering effects due to L, R, and C in traditional packaging technology. Rework of a faulty module can be accomplished by removing the interconnect structure, replacing defective chip, and repeating the fabrication process. High density, reliability and performance are some important features of overlay technology.

2.3 Classification of Packaging Technology

Identifiable interconnect and packaging technologies have evolved out of the ongoing revolutionary activities in electronic packaging industry. These technologies are frequently referred to three categories in accordance with the mounting type, substrate material and construction, IC packaging technique, and pitch size, etc. They are insertion mount, surface mount, and multi-chip module technologies. All IC chips are packed in insertion mount technology. Multi-chip module is a bare chip technology, i.e. an IC chip is unpacked. Surface mount technology, until recently, could be a hybrid of packed and unpacked chip technology. Description of each technology and its characteristics are briefly presented in the following sections.

2.3.1 Insertion Mount Technology

In insertion mount (IMT) technology, that all components and connectors have pin-like leads that are mounted through the hole on the side of printed wiring boards. The opposite board would be in contact with solder in a wave soldering process. All active components of IMT have packed IC chips with long wire lead extensions. Through hole components are first inserted into a board, and then followed by wave soldering to finish attachment of the lead to the hole barrel or the conductor pattern on the opposite side of the PWB. Selected parts and components should be so spaced and so located that any part can be removed from the PWB without melting the solder connection of their neighboring parts.

Selection of components are determined by type of component packages involved, available equipments for mounting, desired size and weight of system, and, of course, cost consideration. Lead shape should also be considered in choosing components. Leads may be attached to unsupported printed conductor lands by clinching or straight-through (unclinched) lead attachment. The lead-to-hole clearance must be enough to provide good soldering conditions.

The most advantage of using the through hole mounting method is its cheaper components and conventional mass solder techniques, such as dual-inline packages (DIP) and wave soldering. IMT is the most matured technique, and most widely used in low-end electronic products. Compare with other mounting technologies, it has a few unavoidable disadvantages that prevent its application in the ever increasing competing electronic markets. First, all the through-hole components are much larger and heavier than other type of components. The PWB can only be mounted in single-side, as one side is used for components and another side for solder connections. Since the component leads are long and flexible, they make components harder for storage, and for assembly process. In a manufacturing assembly process, the component vertical insertion step is difficult to control for avoiding misalignment. This can be caused by prebedded lead, defective through-hole drill and board finish, or warped PWBs. The wiring line pitch is large, due to the nature of insertion process. Electrical performance is poor, because of the parasitic capacitance on inductance in the chip leads, the resistive losses in the board wiring, the induced noise in interconnect, and transmission line effect.

2.3.2 Surface Mount Technology

Surface mount technology (SMT) derives its name from the way its components are attached to PWBs. SMT presents distinct advantages to the manufacturer who needs to reduce product size or increase product functionality. In SMT, active and passive components are packed in a variety of shapes, sizes, and configurations, but with one common feature among them. The common feature is that they all mechanically attached and electrically connected to PWBs through their multiple coplanar leads soldered to match the coplanar pads on one or both surface of the PWBs. Solder, in form of both mechanical integrity and electrical connection, is generally applied to PWBs and/or components prior to position components. Solder is then melted and shaped to its joint configuration in an infrared solder-reflow process.

Components used in SMT are much smaller than those in IMT. Components lead terminal served as both mechanical and electrical attachment. Two general groups of terminals are used: leadless or leaded. Selecting proper terminal type is important for a reliable SMT device. An ideal terminal should be strong enough to withstand routine handing, and yet compliant enough to ease the CTE mismatch of materials. Vias, used in SMT, are smaller than the holes used to hold component leads in IMT. More vias can be used to connect layers and dissipate heat. Three types of vias are usually applied: plated through-holes (PTH), buried, and blind vias. They can be drilled either mechanically or with laser.

SMT assembly results in less PWB layers, less PTHs, smaller pitch size, shorter and less interconnections, less weight, less volume, and higher integrity. All these features contribute to a higher reliability and a better electrical performance. However, heat density is a dominant thermal problem in SMT. Compared to active IMT components, active SMT components have a smaller body size, but dissipate comparable amounts of heat. Another important issue is the design of component pitch size. Though the smaller pitch size the better, yet thermal management, accuracy of placement, soldering, testing and rework capability have to be compromised for a cost effective design.

Unlike earlier technologies, SMT requires a start-to-end involvement of all divisions in production. Team engineering plays a very important role in the achievement of a successful product design in SMT technology.

2.3.3 Multi Chip Module Technology

Multi chip Module (MCM) may be considered as a module or package capable of supporting several chips on a single package. Use of MCMs in many applications reduces volume and weight, improves circuit performance, reduces the number of parts to be assembled, reduces interconnections at PWB level, and hence increases reliability.

MCMs can be subdivided into three categories according to their substrate materials and construction techniques: MCM-C (multilayer ceramic), MCM-L (laminated) or MCM-D (deposited thin-film).

MCM-C substrates are cofired multilayer ceramics. Each layer is patterned with metal wiring for routing interchip connections and connections to module I/O pads. Chips are bonded to the top layer of a multilayer ceramic substrate. Ceramic modules are constructed using layers of "greensheet," which is a mixture of ceramic and glass power suspended in an organic binder. Due to the mechanical properties of ceramic, the advantages of MCM-C include excellence dimensional stability, high reliability, and module power dissipation capacity. The disadvantages include high dialectical constant, limited line and I/O density (compared to MCM-D), and relatively high cost.

MCM-L substrates are fabricated of conventional, and/or newly developed reinforced or unreinforced organic materials using conventional substrate. MCM-L is essentially an extension of PWB technology to finer line widths. MCM-L substrates can provide line widths and spacing as fine as 75 microns (3mils). MCM-L is the most cost-effective technology for an application which do not require very large routing resources, or demand very high performance. The disadvantage is that thermal performance is poor in MCM-L, due to the lower thermal conductivity of the substrate. Substrate cost increases significantly as line widths become finer.

MCM-D substrates are constructed by using silicon, ceramic, copper, or metal composites as basic substrate. Onto this basic substrate, signal and ground conductors are added by sequentially building up layers of unreinforced dielectric materials. Vias are added by fine line lithography, and sputter or plated thin-film metallization processes. The advantages of MCM-D include low dielectric constant, high capability of line, and I/O density. Since the laminated layers have to be processed one-by-one, it attributes to longer process time, and possibly, lower yield. Other disadvantages include limited size of substrate, and high cost. These are due to the lack of vendor infrastruc-

ture and the high cost of process and materials.

Chapter 3

Electronic Product Design Process and Considerations

3.1 Product design process

The design and manufacture of a modern electronic device involve complex process. It is convenient to divide the design process into pre- and post- prototype design stages.

3.1.1 Pre-prototype design

1. **Initial conceptual design phase:** A list of specifications or requirements is usually developed in the concept phase of design, in order to provide a functional description of a product. Depending on the applications, trade-offs are made among packaging techniques, performance, and reliability. Before a new design concept is accepted, following information are carefully reviewed:

Design complexity. It includes how much new design aspects will be added to the previous design, or how much modification will be made. Design issues and experiences of the previous product design are reviewed.

Time to market. The time, needed for design, prototyping, testing, manufacturing, is a key design consideration for a successful product development. A couple of weeks delay would result in the loss of market share.

Cost of the product. Cost issue is also an important factor concerned throughout a product development cycle. It includes the cost of engineering time, new material, new

testing equipment, and robotics machine, etc.

Market share and technology maturity. A product can not survive without a good market prediction. Product design is a market driven process. The needs and shares of market are the major incentives for a new product design. The technology selected for new product is primarily based on its maturity. New technology may provide better performance and options, but may take more time and cost in practice.

Parts availability. Parts used, or may be used, are carefully reviewed. Parts vendor, cost, availability, specification, size, and reliability are studied before a new design started.

Testability, maintainability, and supportability. Generally speaking, every new product acquires new test equipments and maintenance facilities. Issues of linking current product support infrastructure to the new one are addressed in this step.

2. Electrical function design: An electrical design starts with circuits design. Based on the new design requests, a schematic, or logic, diagram is created for electrical functions and interconnections. The schematic defines critical circuits area, shielding, grounding, power distribution, testing points, and signal I/O connectors. Noise, signal to power ratio, path length, and impedance match are the major design parameters in an electrical design. The most difficult aspect of electrical package design is understanding the generation of unwanted signal and noises, and their impact on the overall circuits. Since different types of substrates have significant impacts on electrical performance, the selection and design of a substrate are performed on this stage. In final stage of electrical design, a component list is generated. For every electrical functional module created in schematic diagram, a component (part) is linked with it from a components library.

3. Geometry layout design: Sometime, it is also called product physical design. Design drafters will design a substrate based on a given electrical schematic diagram and a component list. The substrate should have right shape and size that will accommodate

all components and fit available space. Specific design parameters regarding widths of conduction line, space of component, some critical line distribution, via size and location, type of electrical interconnections, and method of soldering are constrained by electrical design parameters. Heat density, heat remove capability, parts placing tolerance, manufacturability are also important parameters in the product layout design.

3.1.2 Post-prototype design

Prototype testing and evaluation: After prototype, an in-depth review is made upon completion of design. The following issues will be determined by electrical and mechanical tests:

•Does it implement the desired electrical functions?

•Are signal distortion and noise in design tolerance?

•Have all dimensional constraints been observed?

•Are leads correctly aligned with land patterns?

•Are solder joint formed correctly?

•Is there any “hot spot”?

•How is mean time to failure(MTTF)?

•How is the reliability in conceivable environments?

•Is there any pre-matured defects?

•What is its yield?

Both electrical and mechanical verifications are involved in this stage to ensure the quality and reliability. The testing results provide useful information for any failure mode analysis and appropriate design modification, if necessary.

Failure mode analysis: A failure mode has to be totally understood before starting any design modification. The analysis may require an intensive analytical, but more practically, a complex computational simulation process. Failure modes include

both electrical and mechanical. But in this stage, it is primarily mechanical. This is because mechanical analysis and simulation are difficult to perform before a product being physically developed. Common mechanical failure modes may be:

•Force and/or temperature induced elastic deformation.

•Yielding

•Ductile rupture

•Fatigue (low- and high- cycle)

•Corrosion (chemical, galvanic, hydrogen, oxygen, pitting, etc.)

•Wear (adhesive, abrasive, fretting, etc.)

•Creep

Product modification: This is the last step in the product design process. However, it may be, again, followed by testing, analysis, and modification, until the quality and reliability have been reached the level that would ensure product competition and customer satisfaction.

3.2 Design considerations

Electrical, mechanical and thermal considerations are the most important design aspects in the scope of the development of an advanced electronic device. There are design issues to current electronic packaging system, for which some design consideration and guideline, standard have been established and others that are still in development. Therefore, it has become necessary to determine and resolve these considerations before the full scale production.

3.2.1 Electrical design consideration.

Number of signal layers in substrate: The decision on number of layers will be

influenced by the degree of crossover of connections and density of interconnection on the substrate. It is the compromise of degree of isolation of one interconnection from another versus the need to get a large number of interconnections in a given substrate.

Digital system interconnection: Digital designer has to consider analog effects in order to cope with today's complex electronic equipment. Transmission line stubs, interlayer vias, voltage mismatch reflections, conductor geometry, and substrate dielectric effects are some of the many factors which demand attention earlier in a system design cycle. The design of high performance digital systems requires the match among system architectures speed, the interconnect, and packaging integration level. In order to maximize the performance and reliability, the following have to be minimized: voltage mismatch reflection, crosstalk between neighboring signal lines, chip-to-chip interconnect delay, signal edge-speed degradation and attenuation, power and ground noise, etc.

3.2.2 Mechanical considerations

Mechanics of material: The materials widely used in a production design includes metal, alloy, polymer, ceramic, composite, crystal, metal, amorphousandn elasomer, etc. The wide variety of materials places a serious analytical responsibility on a designer when material properties are important. The mechanical and electrical properties vary widely over temperature and loading ranges. The first step in the selection of a material is to thoroughly define its service requirements that must be met, such as environment, vibration, g loading, shock, impact, and physical and electrical requirements. The material should be easily available in the form and size required. The material tolerance should be verified according to the needs, and a complete analysis should be performed. The items to be considered include: machinery process, process cost, heat resistance, thermal stability, mechanical strength, electrical properties, flexural strength, CTE, thickness tolerance, ductility, hardness, toughness, fracture strength, safe operating temperatures, etc.

Mechanics of structure: The structure of advanced electronic packaging system serves both electrical interconnect and mechanical support. It is essential that the designed structure of a system is sound and reliable in the required service environment for its life time. Their structural configurations should be carefully designed based on their operating loading, and manufacturing handing and process. The following listed structures are commonly used in electronic products.

- •SMT lead frame structure (J, gull, leadless)
- •Footprint (rectangular, teardrop)
- •Solder formation (concave, convex)
- •Housing structure
- •Via structure (PTH, blind, buried)
- •Component location
- •Support structure
- •Interconnection structure
- •Substrate structure (multilayer thin film, multilayer thin film PI/Metal, FR4 laminated, FR4 HDI laminated)
- •Chip-to-Substrate bonding (WB, TAB, Flip-chip, Overlay)
- •Module-to-substrate (SMT, IMT, BGA, PGA)

3.2.3 Thermal considerations

Heat density is a dominant problem in an advanced packaging device. Compared to active IMT components, today's active components have smaller body sizes, but dissipate about the same amount of heat. Smaller body and large scale system integration increase packaging efficiency and electrical performance, but, consequently result in higher heat densities. The concentrated heat in systems and components has a direct impact to the system performance and product reliability. Statistically, about 50% of overall stress can be attributed to heat temperature, and 30% of system failures are

related to heat concentration. Therefore, heat management is the dominant design aspect in designing an electronic product. Today, as size continues to diminish and power continues to rise, both passive cooling and active cooling system are become more commonplace. The following are common methods used, in mechanical design aspect, to dissipate heat:

Component location for optimum heat transfer: Higher power chips can be diversely relocated, or they can be located to a place that permit better heat transfer, such as PWB edge.

Heat sinks for individual components: thermal conductive pad, or thermal conductive adhesive are used beneath a hot component to support a poor thermal condition with a far better thermal conduction medium.

Cooling plungers: The computer industry has used an array of large, spring-loaded thermal conducting plunders pressing directly against hot individual device, as a way of dissipating extraordinary amount of heat for high performance machines.

Component thermal pads: The thermal transfer from chips, junction through component body into substrates, can be aided by the addition of thermal pads on bottom surface of component.

Thermal vias: Thermal transfer through a PWB into a heat sink can be improved by the addition of extra PTHs in the PWB located in alignment with the component thermal pads.

Heat pipes: heat pipes and hollow-core laminated materials, as heat sink, are used in air or liquid force cooling system.

Chapter 4

Current state of Mechanical Analysis and Modeling

Thermal and mechanical issues of electronic packaging have been widely investigated in different levels by different tools. “Design for reliability” and “cost reduction” are the most prevalent topics addressed in research papers and product design processes. The research areas involved can be generally classified as:

In mechanical design analysis

•structural analysis, stress analysis, vibration, dynamic impact.

••Thermal design

•heat generation, heat remove, cooling capability.

••Material selection

•solder alloy composition, lead material, encapsulation compound, polymer, ceramic.

·In reliability prediction

•fatigue life, crack initiation and growth, creep time.

••Process simulation

•epoxy curing time, oven temperature profile, process control, component handing.

••Optimization

•reduce “time-to-market”, best-pick, cost vs. performance.

An appreciation of all these effects is necessary, and some significant conclusions and suggestions are summarized:

Impact of structure geometry on reliability: Many studies have been made of

the effects of geometry on reliability[13-17,30,33,34,42,44,54,55]. By simply modifying the geometry of a chip housing structure[4, 15] could significantly increase the housing strength and reduce the size needed for packaging. A study of the effect of lead coplanarity and fillet dimension on thermal fatigue life is being carried out by Keegan[8]. This study shows that the lead and solder shape have a large effect on fatigue life. Fatigue life may be improved by a factor of five if lead and solder shape are well designed. A FE analysis of TSOP [11] indicates that solder joint reliability can be improved by a thinner chip, longer leads, more encapsulation, and a single side assembly. A design model for through-hole component presented by CALCE center[5] shows that the fatigue life of the leads in a through-hole package not only depends on the external loads applied to it, but also on the geometry and material properties, architectural parameters of the package, and PWB. In a comparison study of choosing TSOP and PQFP[41], Lau and Golwalkar show that solder joint reliability is a function of the following variables: IC component geometry, material, lead geometry, material, PWB material, thickness, solder joint geometry and mechanical properties, etc. While increasing solder joint thickness in s high-strain condition may improve the reliability of a solder joint, decreasing the solder joint thickness in s low-strain condition may also improve its lifetime. Effect of locations and configurations of vias in cofired ceramic packaging is examined to provide recommendations on a via placement. An Shadowed morie experimental work conducted at Georgia Tech[69] indicates that PWB warpage may be minimized by changing structural configuration and copper distribution in PWB.

Material selection for reliability: A thermomechanical study[46] of thermally conductive adhesives used to attach MCM is presented by Parkash and Wang. It suggests that both thermal and mechanical properties of a material candidate be at concerned in the design of a MCM for good cooling efficiency and strong bonding structure. This is because a decrease in the adhesive layer thickness for a better cooling would result in an increase in stress level as a penalty. In a study of the effect of

different metallurgist, [42] two different BGA sphere metallurgies(90/10 Pb/Sn and 62/36/2 Sn/Pb/Ag) were evaluated. The results show that joint metallurgy, geometry, and height can reduce the effect of CTE mismatch, and so prolong the fatigue life. In order to select the right substrate material for a MCM technology[7,12], thermal performance of a few common materials, such as Si and Ag Epoxy, were evaluated under some hypothetical environments. Because of the sensitivity of the MCM lifetime to thermal performance, a thermal simulation is greatly needed for a better design[18,47,50,51]. According to Solomon's isothermal fatigue data, the average thermal fatigue life of TSOP will increase by 53% if lead frame material change from Alloy 42 to copper. This is due to the smaller CTE mismatch and greater compliance of copper leads. In recent Chip-On-Board technology, Lau[19] indicate that careful selection of substrate material is necessary to ensure its reliability.

Reliability analysis and prediction model: The electrical and mechanical integrity of SMT interconnections depends on the integrity of component solder joints. Overall reliability of SMT is, therefore, almost solely dependent on the overall reliability of SMT solder joint connections. Failure mechanism and fatigue life of solder[1, 21,24,29,42,60] is of prime interest. Several fatigue damage mechanisms exist in solder joint indicating the propagation of a crack, wedge cracking at a grain corner, and gain cavitation. It has been commonly accepted that fatigue crack initiation and growth is the dominate fatigue mechanism. A number of fatigue life prediction models have been proposed:

· Crack propagation & fatigue life model [Coffin and Manson]. It is found that low cycle fatigue data for many metals may be fit to the empirical plastic-strain life relation.

· Strain-life relationship. Engelmaier proposed a Coffin-Manson type relationship for near eutectic SN-Pb solders which includes an empirical description of the effect of cyclic frequency and mean temperature.

· Energy partitioning approach. This approach was proposed by Dasguptal et al. The advantage of this method is that it includes both strain and stress information in life prediction. Dasguptal indicates that power-law relationship between strain range and life also implies a power-law relationship between energy density dissipated per cycle in fatigue life.

Modeling Method: Finite element modeling is the most popular method used to address a design problem. Due to the complexity of electronic packaging structure[35,43,44], FEM is only applied to a small scale or part of the structure, such as a single lead, or a single component. Recently, a few authors have developed new approaches integrating some other techniques into standard FEM to model a more complex problem[45]. Godfrey[9] presents a method on how to solve a 2D temperature profile of a board with a few chips by FEM within a controlling algorithm. In this algorithm, a decoupling algorithm is utilized to eliminate repetitive numerical model generation. A Multi-Point constraint method[10] is used to model a PQFP component with leads. Significant savings in model size and execution time are found compared to standard FEM technique. A global-local procedure[38, 39,40,65], which integrates automatic geometry discretion, auto mesh, and adaptive mesh is presented by Shepard et al. This methodology is considered to "support the reliable integration of global/local thermomechanical analysis for MCMs in a seamless design environment."

Part II

Development of Modularized & Parametric Modeling Methodology

The proposed modeling methodology is developed in this part of the thesis. Identified limitations and needs in mechanical design of electronic packaing are presented in Chapter 5. In order to overcome the limitations, a new modeling approach is developed in chapter 6, 7 and 8. Chapter 6 shows how to define modularized models, and how to assemble the mechanical FE models for an electronic product. Chapter 7 shows how to create and develop a parametric FE module to perform one-to-many modeling and analysis. Chapter 8 develops a new modeling approach for a multilayer PWB substrate.

Chapter 5

Current Limitations and Future Needs in Mechanical Design Analysis

Based on the literature review in part I and the research study of mechanical design analysis activities in the current product design environment, the identified limitations and needs for rapid mechanical design are presented in this chapter. In the first section of this chapter, three mechanical design obstacles are discussed. These obstacles include the complexity of conventional FE method, the lack of product design-data sharing capability, and the limitations of current mechanical modeling capability. In the second section, the needs for improving current mechanical design are suggested. The thesis goal and objectives are presented in the third section.

5.1 Current Limitations in Mechanical Design Analysis

Three major limitations are existing in a general product development cycle. First, it is hard for an electrical engineer to perform thermomechanical design. second, it takes a mechanical engineer too much time to find the needed information and perform a mechanical analysis. Furthermore, the mechanical design and modeling capabilities are greatly limited by currently available methodologies.

5.1.1 Complexity of Conventional FE Method

The generality and versatility of the FEM enable an engineer to tackle complex

engineering analysis problems, but its usefulness and efficiency are largely depend on a designer's experience.

The FEM is a piecewise approximation method, in which the approximation function is formed by connecting simple functions. The finite element procedure produces many simultaneous algebra equations. They are generated and solved on a digital computer. The produced results are rarely exact. However, errors are decreased by processing more equations. The desired degree of result accuracy is depend on the need of modeling at reasonable cost. A finite element analysis typically involves following steps:

1. Problem Definition for a requested analysis. It includes making assumptions, selecting analysis types, and eliminating unnecessary details.
2. Modeling a given 3-D geometry, constructing an appropriate FEM model from the given object model as per the problem definition;
3. Analysis type specification, providing all details, which are necessary for the particular type of an analysis;
4. Discretization of the FE model, discretizing the entire FEM model into a properly connected mesh of suitably sized and shaped elements;
5. Applying loads and boundary conditions, assigning loads and boundary conditions to particular nodes of the mesh;
6. Analysis the loaded model, carrying out the FEM solution using a code-solver;
7. FEA result interpolation, assessing the validity of the results;
8. Repeating the steps 1-6 until acceptable results are obtained.

Problem definition, in step one, is primarily based on the understanding of a given problem and the knowledge on the mechanical field for that particular problem. The typical questions have to be answered, in this step, include: what is the failure mechanism? is it due to a thermal, or structural, or vibrational load, or their combination? is any part can be ignored or simplified? is the model applied for quantitative or qualita-

tive? how much accuracy is desired? This is the foremost approximation step of a FEA process, and has a great impact on the quality of analysis performed later. Without an appropriate approximation for the problem, the final results would either be misleading or error prone.

Step 2 is the process where geometry is defined in a digital format. Sometime, it is called as solid modeling process. However, unlike a traditional solid modeling process, the geometry attributes have to be customarily decomposed for an easy meshing operation. This is because simply creating a geometry model, by Boolean operations or primitives modifications, would result in generation of poor quality mesh, and sometime, the impossibility of performing a solution. There are no general rules on how to decompose a geometry, and to represent an attribute. Rules are varying in different problems, and are dependent on an engineer's experiences.

After the geometry is built, the material properties and the physical properties are assigned to the geometry attributes. Using linear or nonlinear analysis has to be determined. Often at a time, some material properties may not be available, an approximation and a literature search for the needed material properties may be required.

Step 4 is generally the most difficult and time consuming part in a FEA procedure. It involves two substeps, which are selecting appropriate element type and meshing the geometry attributes. The decision of choosing an element is not a simple task. An element that is good for one problem, may be poor for others. Even in a specific problem, an element may behave differently, depending on the particular geometry, loading and boundary conditions. A FEA user has to familiar with how various elements behave under various conditions. The second sub-step is to mesh the geometry attributes. To generate a mesh for a given geometry is difficult, and dependent on experiences. The density and the shape of elements are the primary concerns. The questions, such as how much elements are enough, how small an element is small enough, and what is upper limit of the aspect and distortion ratio of an element, are impossible to

answer without a specifically described geometry in a specifically defined problem. Creating a good meshing result is indeed not an easy task.

After the geometry model is meshed, the loads and boundary conditions are added to the model. Two types of loads have to be included. They are constraint loads and external force loads. Constraint loads are generally refereed to as boundary conditions. It eliminates a rigid body and translation motion, and describes the physical properties of its boundaries. The external force loads may include any combination of external forces, such as temperature, and body force. They are applied to simulate the actual environments. Different load steps and load forces may be "ramped or stepped" in the solution process. The application of adding the loads on the geometry attributes is the part of a FEA model, and is subject to assumptions and approximations applied on the model.

Step 1 to 6 fully develop a FEA model. The solution of a FEA model can be easily performed by a digital computer. Convergence and actual physical representation of the solution have to be checked during and after the solution process. Since the element density and convergence criteria may not be defined well in the model preparing process, a few more iterations, from step 4 to 6, may be required. After the convergence is confirmed, the solutions are compared with actual physical problems. Because FEA is an approximation method, without good understanding and interpolation of these obtained calculation, the solution results are meaningless.

Because of the nature of FEA methods, mechanical knowledge and FEA programming experiences are required throughout the entire procedure. This makes it difficult for an electrical engineer to perform a thermomechanical analysis in a product design process. Besides, there are more reasons that make FEA impractical within an electrical design. First, FEA is very time consuming. It may easily take an experienced mechanical engineer a few days, even weeks, to perform a finite element analysis. Second, the component geometries and material properties are not evidently visible during the design

process. A FEA can not be performed without these information. finally, even after all these information are available, transformation of the data from an electrical design environment to mechanical could be another arduous and time consuming process.

5.1.2 Lack of Design Data Sharing Capability

The integration of multi-disciplinary processes of an entire product development is highly dependent on the communication of data, which includes all information associated with the product. The dataflow includes the information generated from components (parts) vendor, component library inventory, electrical design tools, physical design tools, thermomechanical design tools, and manufacturing process. The components and product related data, currently, can be only transferred within a single disciplinary design environment. When it is transferred from one disciplinary tool to another, a special translator has to be used for either filtering or mapping the data from one format to anther. During the translation, the part of product information is lost. Some of them can not be recovered, but they could be very valuable for later designs and analyses.

Information Provided by Component Vendors: When a component vendor fabricates a component for an electrical product. All the information associated with this component are clearly described. It includes detail 3D geometry information, fabricated materials, mechanical and electrical properties, electrical specification data, and the cost. It is important to note that there are component standards in the electrical component industry. These standards have the feature definitions for geometry shapes and/or electrical performances. In general, component vendors maintain their product catalogs, for customers to select their product by geometry, performance, or environment requirement.

Information Generated in Electrical Functional Design: In order to achieve the automation of an electrical design process, the electrical design tool companies, i.e.

Mentor Graphics and CADENS, have constitute their electrical component library as part of their software package. Inside the library, components are categorized by electrical performance, specification, mount type, land pattern, lead type, etc. They are used for electrical designs and component selections. The information contained in the library is from the component vendors. When new components are needed, the component library may be independently updated, rather than updating the entire software package. This library may be further directly linked with different vendor's product catalogs. This link provides one-to-many mapping relations. Thus, when a component is not available at the time of manufacturing, an alternative component can be found for replacement. Though the build-in component library provides so much advantage, it has a critical disability. It does not contains most of detailed mechanical information. This is because only a part of component product information is filtered and transformed into the library. The reason is believed to be that the electrical fuctional design is the only emphasis for these software package.

Information Generated in Product Layout Design: Electrical functional design produces electrical schematic and interconnection diagrams. These information are passed to mechanical (electrical) engineers to perform a physical design. Usually, the physical design is performed in a different software package. Though the electrical functional design tools can output the geometry information, most of them are 2-1/2 dimensional. That is, only the 2D projection of each layer is showed. Component's height and lead geometry are not available. For a PWB, the information of each substrate layer are separately produced, only land pattern of each layer are visible. Via structures can not be seen by looking at each single layer geometry. In order to produce the 3D view of a PWB, each layer has to be manually stacked-up. In such a process, the transformation of design information is processed half-automatically. More important, the concept of component attributes is lost. The component attributes are represented by wire frames or surfaces in the electrical layout design. Thus, the query process, such as

“give all the geometry information associated with T34 component”, can not be performed. When a mechanical designer wants to do an analysis for that component, the geometric information of the component can be hard to retrieve. Though some of electrical layout tools and physical design tools produce data in STEP format, such as AP203 and AP210, they are not easy to use for the mechanical design and analysis. The contained information, in STEP, are better designed for manufacturing (geometry emphasized), and are in short of the information needed for thermomechanical design, such solder joint formation and material properties.

Information maintained by System Manufacturers: The general strategy for component selection is to select the smallest quantity, fewest part types, and fewest vendors. The commanding imperative for component selection is to select only the parts with company-documented packaging specifications, including material, placement, reliability and soldering process requirement. In order to achieve this, most of the large semiconductor companies maintain their own component libraries for qualified components, based on the performance, reliability, and cost. These libraries include electrical specification, 2D land pattern geometry, mounting type, vendor's name, cost, quality, and reliability data. These information are used as design guidelines for each new product development. This database, sometime, can be linked directly with an electrical design software, as to select appropriate components for an electrical function deign. The information contained are primarily filtered from vendor's product catalogs and previous design experiments. However, the detailed geometric attributes and thermomechanical design information, once again, are ignored.

Information Needed by Mechanical Designs and analyses: Even inside a mechanical design environment, there are significant gaps between design tools and analysis tools. Most of the design software, such as I-deals and Pro-E, are primarily used for geometrical visualization and manufacture. They are solid modeling tools, and have very little capability to perform a thermomechanical analysis for a mechanical design

and process. The mechanical analysis tools, such as ANSYS, ABQUAS and DYN3D, are focused on solving numerical models. Though they can address multi-disciplinary problems, like structural, thermal, and even dynamic problem, the time for model generation of a specific problem may take a long time. There are difficulties to transfer a solid model from a design tool to a analysis tool.

It is noted that each product development step has ignored "unrelated" information, in order to simplify and optimize its own process. Electrical fuctional design tools filter out 3D geometry and material information, and only keep the data for electrical information and basic land pattern descriptions. The physical design process only captures pure geometry descriptions, while component attributes, material properties, and object hierarchy information are ignored. The entire product information is spread out and shared in different developing environments, database systems, and data format. A designer could only retrieve a part of product information inside his working scenario. Consequently, the backup of needed information would be a hard task, especially for a mechanical designer when a thermomechanical problem is to be addressed. For example, when a manufacturing or testing personnel come a mechanical designer, and ask for a solution, only general product descriptions and its problems can be presented. The mechanical designer has to go through all the development team himself, in order to obtain all the needed information to perform a mechanical analysis.

5.1.3 Limitations of mechanical modeling

While rigorous thermomechanical modeling and analysis have been applied to electronic packaging to provide a greater understanding of the physics of the problem, a few issues and limitations are observed and in need of improvement:

- **Only by expert.** Accurate solutions can only be obtained by experts who use numerous iterative simulation runs for 2D and 3D mesh models.
- **Repetitive in nature.** Similar structures have been remodeled for same/different task.

For example, determining an optimal PWB design typically requires modeling and analyzing several different chip configurations. At present, much of the time and cost spent modeling these various configurations is repetitive in nature, with the same chip or board being regenerated several times before obtaining the a more efficient design.

- **Simple configuration.** Packaging structure is often reduced for easy modeling. for example, PWB is regarded as uniform; 3D structure is reduced to 2D
- **Single part.** A modeled part is not changed, regardless of location and orientation, such as a lead in different location of a TSOP, and a chip on different site of a board are same.
- **Time consuming.** Models are always started from scratch.

5.2 Future Needs for Concurrent Mechanical Design and Analysis

The design of an electronic packaging is the science and technology that involves many disciplinary, such as electrical engineering, mechanical engineering, chemistry, applied physics, etc. To stay completive in the market, this complex interdisciplinary activity requires the participation of all disciplinary personnels with design engineers, so as to create a successful solution for a new packaging application. The integration of multi-disciplinary technologies throughout the design and analysis involves significant sharing computer based information. This section will discuss some needs in electrical and mechanical design areas. These needs include: integration of E/MCAD; Integration MCADs with analysis tools.

5.2.1. Integration of E/MCAD for current design.

Concurrent design, is also called team design, which means people from all disciplines get involved early, and together to launch a new product or model.[47] Often times, a product engineer has a wide array of electronic packages to choose for the appli-

cation[3,7,23,52]. The package that is finally chosen is a trade-off of the cost vs. performance. Thermomechanical performance and reliability is one of the important aspects that need to be carefully considered. To facilitate in the thermomechanical performance comparison, every product engineer needs a methodology and a handy tool within the electronic design environment. Today, mechanical design, especially thermo-mechanical behavior design, is typically considered only at the final stage of the design process. Typically, Max. temperature, strain/stress, and cooling efficiency, are needed to be compared under various assumed conditions in terms of the application[50].

Traditionally, a product development process can be described in terms of design-prototyping-testing-modification. Electrical function design is the primary activity in a design process. Thermal or thermomechanical design issues are roughly checked in, or after, a physical design process. Intensive thermomechanical design and analysis are involved, only after problems are observed either on manufacturing line or in reliability testing. In many cases, due to the deadline of product shipment, or the high cost of design modification, only short-term solutions, or no solution, can be obtained at this stage. In order to balance the design requirements and the cost of design modifications, the short-term solutions are obtained by "trail-and-error" methods. Such an approach is often costly and responsible for significant time delay in the development process, and sometime ineffective in assuring product reliability throughout the life cycle. Since the cause of failure may not be fully understood, the same failure mechanism may be appeared again on another new product. Thus, life cycle cost and time-to-market are increased.

Now, in the interests of shorter turnaround time and the need for a single-pass design and manufacturing cycle, mechanical design has to be made up front with other design decisions. This requires mechanical computer aided design (MCAD) tools to be integrated into the electrical computer aided design(ECAD) system[12]. The integration of E/MCAD system may provide a design decision based on an optimum balance among

the many requirements and constraints. With the help of a computer, a numerical simulation can be done in a very quick manner. The simulation may estimate the thermomechanical characteristics of the assembly and indicate the critical component which might be vulnerable under some condition. This information will be very valuable for an effective design modification. Hence, if a numerical solution exists for a given model, experiments test can be postponed until the final design stage[53], leaving the initial design stage to a more effective technique. Concurrent mechanical design, with electrical, may recognize and eliminate the thermomechanical failure mode prior to final product design, and so generate a "failure-free" product which is "correct by design"[4].

5.2.2. Unification of MCAD with numerical analysis tool.

Integration of MCAD with numerical analysis tools is an important issue in design automation. Most of the available MCAD systems are used primarily for drafting, layout and parts lists, but only marginally affect the realm of an engineering analysis[19,25-27]. CAD programs, which are developed by the means of conventional information processing technologies, rely mostly on procedural representation of 3-D objects and do not have the capability to undertake analysis tasks, such as finite element analysis. Although, geometry information "translators" are available among major CAD and FEA software, the product design information, received by a FEA preprocessor through the translators, are hardly able to use. This is because: 1. Only geometry information (wire frame, surface, solid) is transferred, while lots of other information are lost, such as the concept of object attributes, the information of properties, the descriptions of behaviors and functions; 2. Direct transformation of a design geometry, from one CAD package to a FEA software, includes too much tiny and/or noncritical geometries, which make the computational analyses practically impossible.

The gap between the MCAD system and analysis tools led to the emergence of

new technologies into existing MCAD systems. New technologies include knowledge-based engineering, object oriented framework, computer algorithms, and standard definition of product information. The desired system should be able to capture both geometric and non-geometric product information, and to provide different levels of product information. These informations should include: components list; their geometric relation and inheritance hierarchy; geometric information to represent the shape; structural characteristics; information to represent attribute and properties; description of function; engineering judgement and analysis reduction for typical geometry; engineering rules; manufacturing constraints, and so on.

5.3 Research Goal and objectives

The previous sections addressed some problems in the electronic design process, and identified some needs for the current state of mechanical design environments. This section outlines objectives and the organization of methodology development.

The goal of the thesis is to develop a computer-based parametric modeling methodology to perform thermomechanical analyses and simulations in a seamless electronic product design environment. With the help of computational techniques and computer algorithms, the developed methodology can:

- Create analysis models rapidly and flexibly.
- Provide concurrent design capability.
- Perform “what if” scenarios.
- Reduce modeling repetition.
- Generate flexible, transportable, and interchangeable FE models.
- Provide integrated analysis capability.

The research scenarios are focus on the areas of thermomechanical modeling and

analyses for the design analysis of electronic products. In order to overcome the limitations addressed in previous sections, a new modeling approach is developed in chapter 6 and 7. Chapter 6 shows how to define modularized models, and how to assemble the mechanical FE models for an electronic product. Chapter 7 shows how to create and develop a parametric FE module for a one-to-many modeling capability. Chapter 8 develops a new modeling approach for a multilayer PWB. Based on the developed methodology, two case studies are conducted. The first case study, parametric FE modeling for flip-chip on board, presents a systematic analyses based on the predefined parameters. The parameters include geometry size, initial conditions, loading conditions, materials, and optimization criteria. The second case study, MP/FEM for a board-level thermomechanical analysis, demonstrates the capability and flexibility of the methodology in model generation and model solution. A detailed FE model is assembled for a populated board. Different types of analyses, including global/local analysis, are performed.

Chapter 6

Modularized Modeling Approach

The first part of the developed MP/FEM methodology is presented in this chapter. The concepts of geometric decomposition and modularization are introduced in the first section. It is the baseline for developing the modularized modeling approach. Modularized geometry primitives (MGPs) are defined. MGPs are considered as the most basic building blocks for a modeling assembly. In section 6.2, the taxonomic technique is used to classify electrical components into a number of limited categories. The component module relations are represented as a graph tree in section 6.3. The method of how to construct the tree is showed in section 6.4. A mechanical model of a product can be easily assembled based on the developed graph tree. A few algorithms are presented, in section 6.5, for the unitization of the graph tree. Section 6.6 describes how to create the FE model for a MGP. Section 6.7 illustrate the differences between the developed MGPs and superelement. Finally, in section 6.7, a BGA structure is decomposed into modularized FE modules.

6.1 Modularized Concept

6.1.1 Geometric Decomposition

The concept of modularization can be related to a product decomposition. The

purpose of modularization operations is to break a complex physical object into small units, which are simple enough for both mechanical design and analysis. The modularization concept is, however, different than a geometric decomposition. Geometry decomposition breaks a 3D geometry model into smaller attributes, then into simple geometry primitives, like cubic, polygon, line, and points. Geometry decomposition usually is based on predefined generic geometric protocol and boolean operations. In geometry decomposition, there are basic forming rules to define the construction of each geometric object, such as topdown decomposition and bottomup construction. Topdown decomposition implies that the geometry of a product is represented as the combination of boolean operations by using predefined basic geometry primitives. Bottomup is to create the geometry of a product by defined points first, then followed by defined lines, surfaces, and solid geometries. These two geometric modeling approaches may be combined in creating a complex geometric object. Compared to a pure geometry decomposition, each modularized part may still include complex geometry attributes, which are considered as incompleted objects in a geometry decomposition. The "breakdown" process of modularization is an object-oriented process. In addition, it has to be considered as the decomposition of a product to mechanical models, so they can be applied for concurrent design and analysis.

Constructive solid geometry(CSG) is a graph representation geometry structure. It is one of the most popular methods used for representing decomposed geometry entities. It preserves the three dimensional structure of an object and also provides the hierarchical representation. But, the representation is only syntactic. A mechanical model for finite element analysis needs additional information about the properties of its objects, such as topological and physical properties. A modified graph tree, similar to CSG, has been developed to embed both analysis and process information for FEM model development.

6.1.2 Definition of Modularization

A direct way of defining the modularization concept, in the scope of this thesis, is to refer to it as group technology, in which many electrical components and/or products can be grouped into classes or families of similar shapes. Each single family of a topological shape is called a Modularized Generic Primitive (MGP). An individual member of a family can be distinguished by a few parameters. A new geometric shape can be created by linear transformations of an existing one. It should be noticed that such transformations affect the geometry size only, but not the topology of a shape. That is, each MGP is defined by its topology, not by a detail geometric size. For example, the topology of a family of cylindrical objects is defined as a cylindrical body with two parallel spherical surfaces on each opposite side. It may be stretched, or resized (Figure 6.1), but they belong to the same MGP (family).

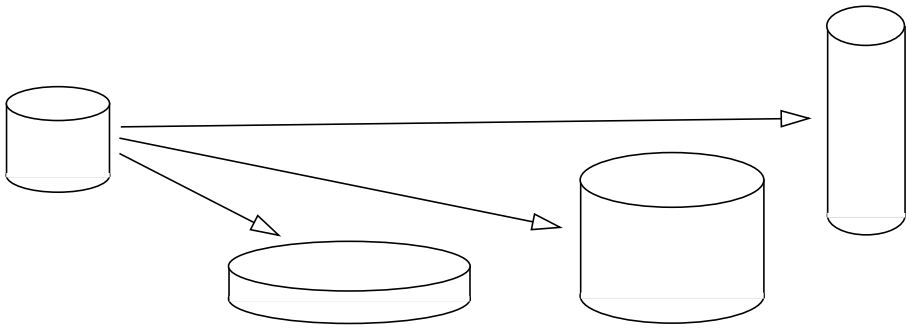


Figure 6.1 Objects of different geometry size with same topological shape.

The modularization concept defined in this thesis is for mechanical analysis. Its operation of modularization is based on the knowledge of mechanical design and analysis. It is intend to break the entire product into small MGPs (modularized parts), so that each MGP can be manipulated in a simple manner. The rules of how to define and operate, are highly dependent on the user's knowledge of mechanical design of electrical products. The knowledge includes the understanding of electrical function and configu-

ration of components, and experiences of performing failure analysis and prediction. The efficiency of applying modularized modeling may be affected by how good the MGPs are created. However, several rules are recommended to achieve desired efficiency and convenience. They are:

Rule 1. Each MGP has to be able to support a number of component shapes, while still maintaining its topology.

Rule 2. Each MGP has to be a 3D geometry object, not a simple 2D geometry object. A 3D model is highly preferred, and no surface MPG. This rule will prevent the decomposed geometry attribute lower than surface (2D) level, such as curve and points. This is because: 1) the 2D model may not well represent the real physical structure, and may be difficult to interpolate the 2D analysis results for a real engineering problem; 2) the 2D analysis is generally less conservative, providing results which may be misleading. This rule excludes the objects that may be modeled as 2D objects, such as 3D layered shelled objects, but it still maintains their 3D behavior.

Rule 3. Each MPG is constructed only by one material. This is required because of the concerns of the physical aspects of components and algorithms of FE mesh generation. A component, which consists of different materials, is generally be able to be decomposed into pieces with a single material.

Rule 4. Each MPG may not be smaller than the physical part attribute of a component. Physical part attributes refer to the smallest part used to bring together or perform a function, either electrical or mechanical. For example, a TSOP component lead frame is regarded as a smallest part attribute of the component, and is not suitable for further decomposition into lead_shoulder, lead_base, and lead_height. Though they all can be represented as 3D solid (thin shell) models, and satisfy rule 1-3, this level of detail may cause construction ambiguity and computational difficulty.

Rule 5. Each MPG must be able to be modeled independently. This is a very important aspect. It is essential that each MGP can be independently constructed and

flexibly meshed. Each MPG has to have the flexibility to refine its finite element mesh when its geometry size is changed.

Rule 6. Each modularized part must have common boundaries to its neighboring parts, and its boundary must be able to be meshed appropriately and refined easily. This rule is primarily for the concern of meshing compatibility at the interface of each part. A MGP can not be attach to another object arbitrarily. Whenever a MPG is defined, its possible attachment construction has to be defined at same time. Its boundaries have to be meshed in such a way, that when it is attached to, or being attached by another part, the compatibilities of nodes and elements have to be guaranteed.

Rule 7. Each MPG must maintain its forming rules and connection constraints, when it is moved or resized. This rule has to be considered when a MGP is initially constructed. The geometry definition of a MPG should not be based on fixed variables. The correlations of variables used to define a MGP have to be linked with other MGPs, so that when its neighboring parts are changed, it may be changed accordingly. The modification operations may be the combination of addition, deletion, duplication, and translation. In the case of a modification, the forming rules and connection constraints should either maintain their old properties, or be updated appropriately. This will require the variables being defined locally, and connection relations defined externally.

Rule 8. Each MPG may be inherited by others to construct a higher level module. The MGPs defined in this research work are the most basic building blocks to assemble more complex components or products. MGPs can not be further decomposed, but can support upward hierarchical construction. For instance, a solder joint and lead frame may be duplicated, and then combined with a plastic body to form a component. This component may be further duplicated, and mounted on a board to construct a board assembly with many components. Since duplication and movement

are heavily involved in constructing a board-level model, the reusability is definitely a big concern in the creation of MGPs.

It is important to note that the methods and rules defined above are primarily for mechanical design and analysis of electrical products in SMT. It is in this area that these rules are believed to serve better ability in the time cycle reduction of product design. Though these methods and concepts may be developed for other products in a more generic scope, they are not studied in this research work. In the next section, the taxonomic technique is used to categorize SMT components.

6.2 Taxonomic Technique

In product design, most products are not started from scratch, but are instead chosen from an electronic component library, which contains a limited number of basic electronic components (functional modules)[59,60-62,64], such as a chip, a resistor or capacitor. Most of the substrate, or the interconnection, can be limited to Plate Through Hole(PTH), Surface Mount Technology (SMT), Wirebonding (WB), Taped Automatic Bonding (TAB), or Flip Chip, Ball Grid Array(BGA). Generally, there are a limited number of components used to fabricate a product, and limited types of interconnections in a component assembly. Based on this observation, SMT components can be classified into categories. In this research work, only SMT components are studied. But same approaches may be extended to PTH and MCM technology. According to the characteristics of geometry and topology of electrical components, the defined categories include: (1)active; (2)passive, (3) chip-level attachment, (4) BGA, (5) footprint, (6) vias, (7) solder joint formation. Additional components, such as switches, fuses, connectors, and lamps, are omitted in this thesis work, because they generally have little design and reliability issues involved in mechanical design scenarios.

1. **Active component.** Active components are semiconductor devices that amplify,

switch, or rectify electronic signals. Transistors and packed components with IC chip are belonged to this categories, such as TSOPs (Thin Small Outline Package), QFPs(Quad Flat Package), LLCCs(Leadless Ceramic Chip Carriers), and SOTs(Small outline transistor). Most of active surface mounted component are available with different termination styles. There are several dominant styles used on leaded packages and one styles on lesdless device. Package material may be ceramic or plastic. They are distinguished for geometric modeling purpose. Leaded terminations are identified by their particular shape: Gull wing, J lead or C lead, and I lead. (see Figure 6.2) Transistors are in the shape of modled plastic package, and specifically designed for non-hemetically sealed SMT application. It is worth-while to point out that most geometry of component types have its industrial standard definition. So it can be referred to further improve the efficiency of taxo-nomic technique.

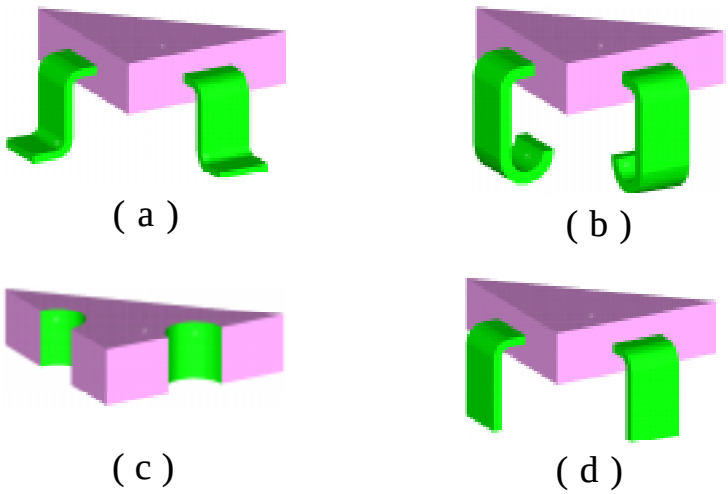


Figure 6.2 Taxonomy of active components. (a) Gull lead; (b) J lead; (c) Leadless; (d) I lead.

For each active component, it will be further decomposed as a body package,

lead frames, and its connecting solder joints. The shapes of a solder joint may vary in different components and soldering process.

2. **Passive component.** Passive components consist of electronic components such as resistors, capacitors, inductors, etc. The geometry shape of a passive component in SMT are fairly simple. They usually are small brick-like cubic, and are often lead-less device. The leadless terminations on passive components, often referred to as "end cap", are formed by first applying a fused, metallization layer of silver, or equivalent alloy. The end-caplayer is then followed by a barrier coat of nickel. A final coat of tin-lead is often applied over nickel for better solderability. Passive chip terminations are available as single-side, three-side, or five-side. (Figure 6.3)

For passive component, it will be decomposed into a cubic body and solder joints on two sides.

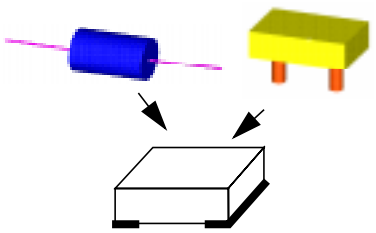


Figure 6.3 Passive components.

3. **Chip-Level Attachment.** Flip-Chip On Board(FCOB) or Direct Chip Attach (DCA)Flip chip on board (FCOB) technology, also called direct chip attach (DCA), or flip chip attach (FCA), has recently received increasing attention as a way to improve package density and electrical performance IC chip with solder bumps is attached to a substrate, usually organic FR-4 board. After solder reflow process, the melted solder serves both mechanical and electrical functions in FCOB assembly. The solder reflow process is followed by underfill process, so as to form encapsulation (epoxy). The geometry of the FCOB structure is shown in Figure. Though the processes of DCA, C-4, SCM have different process and use different materials, they can be treated equivalently in geometric modeling (FIgure 6.4).

For a DCA Assembly, it can be broken down into parts of an IC chip, solder

balls, underfill encapsulate, fillet encapsulant, and corresponding substrate.

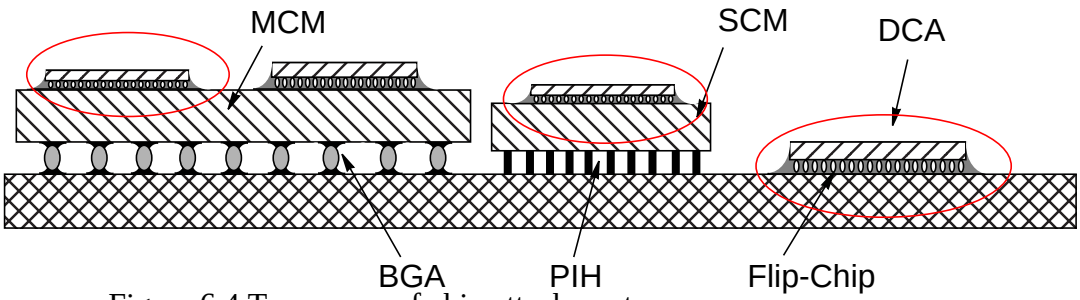


Figure 6.4 Taxonomy of chip attachment.

4. **Ball grid array (BGA).** BGA, which is referred to ball grid array, is second level interconnection in a electronic device. A ceramic module containing one or more chips is attached to a circuit card (FR-4) by means of a array of non-homogeneous solder balls. Theses connections consist of a high temperature melting solder (90Pb/10Sn) sphere attached to the module and card with eutectic solder fillets. The solder structure offer both electrical connection and mechanical support. Three different BGA types are current in practice, Plastic BGA (PBGA), ceramic BGA (CBGA), and tape BGA (TBGA). From mechanical modeling points of view, they can be treated equally.

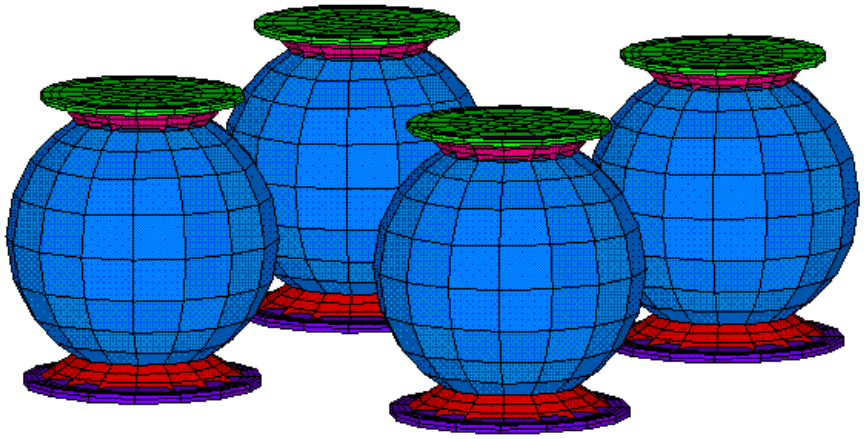


Figure 6.4 Taxonomic technique: Ball Grid Array (BGA)

A BGA structure is broken into several modules for easy modeling. The modules for a single BGA interconnection are: Chip(0-level) substrate, upper solder pad for eutectic solder, upper eutectic solder connection, Non-eutectic solder ball, lower eutectic solder connection, lower solder pad for eutectic solder, and Board (1st-level) substrate.

5. **Foot print (land pattern).** Most common footprint in SMT is narrow squares. It can be used for J-lead and gull-lead device. Some alternative pad patterns are also used to develop fine-pitch and high yield process. They are staggered, inverted triangle, teardrops. (figure6.5) Each pattern may be modeled regardless the attached component, as long as the base of the lead frame of a component match

the pad pattern.

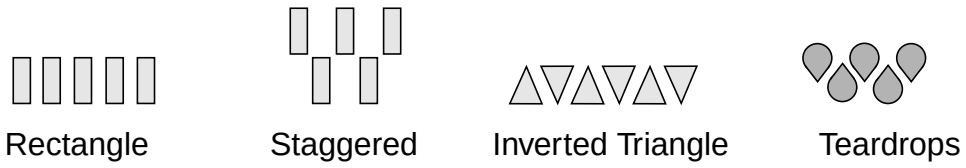


Figure 6.5 Taxonomy of foot prints.

6. **Vias**. Vias, are plate holes, selectively placed throughout the substrate, used to interconnect interplanar circuit conductors in multilayer boards. There are three types of vias: plate through hole, buried vias, and blind vias. (Figure 6.6)

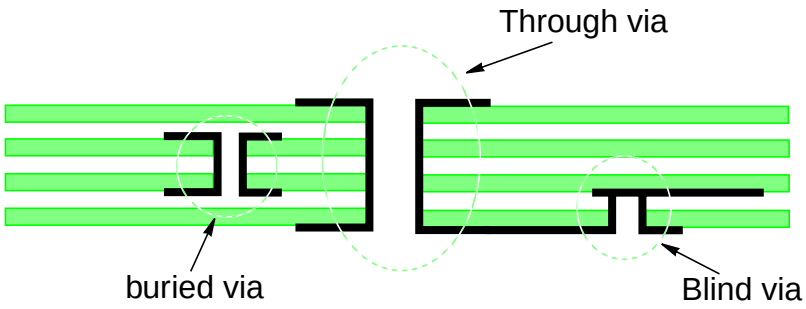


Figure 6.6 Taxonomy of vias.

7. **Solder joint formation.** The shape of final solder joint formation is not available, until the prototype is being built. However, the shape and formation of solder joints have a significant impact on overall reliability of a electronic system. It is important to predict and analyze its structure to ensure the quality and reliability. A few solder profile issues are commonly encountered: variations of solder volume that affect the shape of side fillet (case a, b, c in Figure 6.7); bad alignment and/or solder reflow of components that cause bad solder connection, such as tombstone,

swimming, and alignment (case d, e, f in Figure 6.7); solder volume underneath the lead frame; lead coplanarity that causes poor solder joint formation;

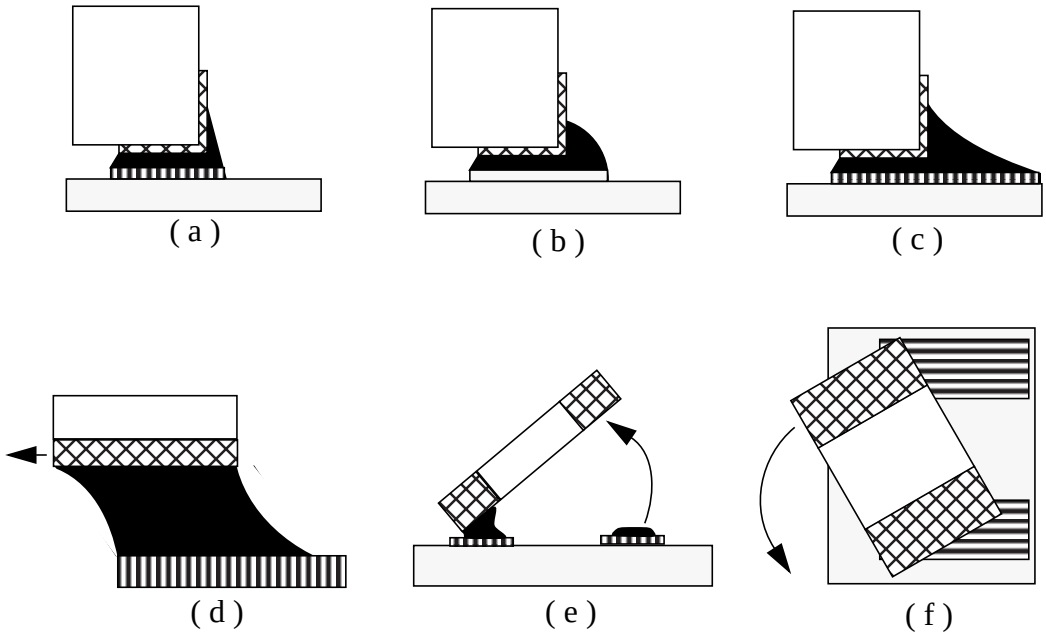


Figure 6.7 Taxonomy of solder joint variations: (a) insufficient solder; (b) optimal solder; (c) excessive solder; (d) mis-alignment; (e)tone-stone effect; (f) swimming.

Though not all the electrical components are included in this thesis, the categories defined here represent a majority of critical components in current electrical products in SMT. The classified categories, as shown above, will not be fully studied. The motivation of the taxonomic technic is to demonstrate that most electrical components can be limited into a small number of categories. These categories can be used to represent most of (if not all) the electric assembly. Once they are investigated in a product, they may be reused for other products with very little effort. Only a number of these categories are fully studied to demonstrate the developed methodology. It has to be pointed out that the components in the categories defined in the preceding sections are not the MGPs. The components in each category will be further decomposed into

smaller pieces, which are called MGPs. As defined in previous sections, each MPG has to belong to one, and only one, component category.

6.3 Module Relation Representation

6.3.1 Graph Theory

The overall relationship among MGPs, components, assembly, and product is represented as a graph tree. This tree is referred as Constructive Module Assembly Tree (CMAT). Before the CMAT is introduced, the notations of definition and representation of a graph are briefly overviewed:

Definition: A graph *G* is a pair *(V,E)*, where *V* is a finite set and *E* is a binary relation on *V*. The set *V* is called the vertex set of *G*, and its elements are called vertices. The set *E* is called the representation of directed graph on the vertex set called edges.

Graph Representation (directed and undirected): A graph can be represented in any one of theses format: pictorial, adjacency-list, or adjacency-matrix (Figure 6.8). The adjacency-list of a graph *G=(V,E)* consists of an array *Adj* of |*V*|, one for each vertex in vertex in *V*. For each $u \in V$, the adjacency list *Adj[u]* contains points to all the vertices v such that there is an edge $(u, v) \in E$. That is, *Adj[u]* consists of all the vertices adjacent to u in G. For adjacency-matrix representation of a graph *G=(V,E)* consists of a $|V| \times |V|$ matrix $A=(a_{ij})$ such that

$$a_{ij} = \begin{cases} 1 & if\,(i, j) \in E \\ 0 & otherwise \end{cases}$$

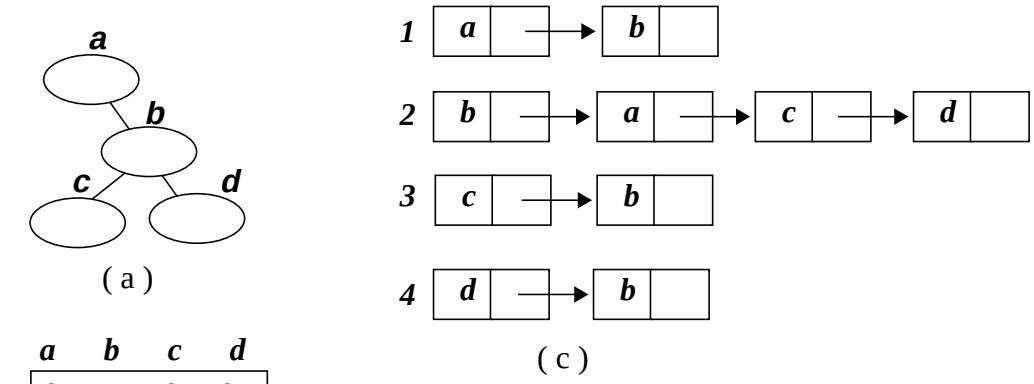


Figure 6.8. Graph Representation. (a) a pictorial graph G with 4 vertices and 3 edges; (b) A Adjacency-matrix representation of G; (c) A adjacency-list representation of G.

6.3.2 Constructive Module Assembly Tree.

The CMAT is an undirected graph, or a rooted tree, where the root is the electrical product itself. It is represented as $G_{CMAT}(V, E)$, where V is the vertices set (component nodes), and E is the edge set that links between the vertices (Figure 6.9). The degree of a vertex in G_{CMAT} is defined as the number of dashed edges that have to walk through in order to reach the vertices from the root. Dashed lines represent decomposition operations, while solid lines level represent a group of parts with same degree. The vertices may be MGPs, simple components, or a very complex product containing many electrical components.

The root node of G_{CMAT}has it is dependents. The edge of 1st-level decomposition is the link of root node to its dependents, which may be many PWBs. The second level decomposition can further break each PWB down into component level. Each

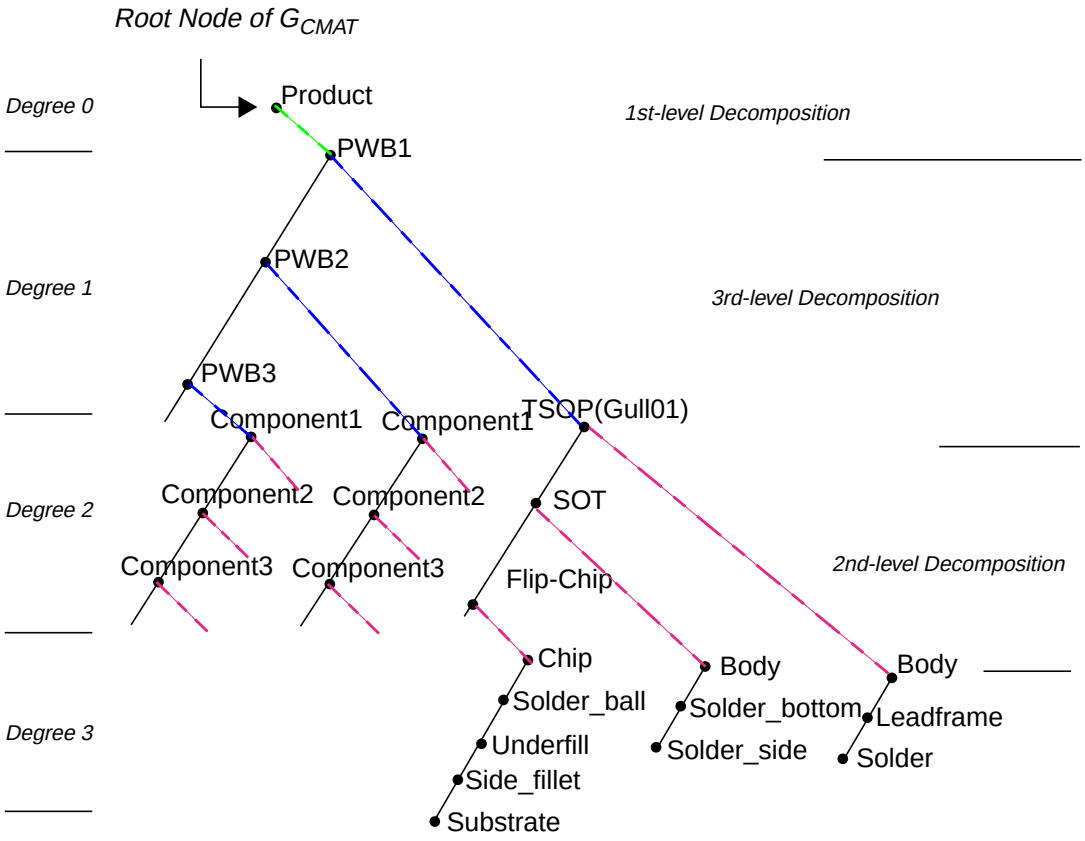


Figure 6.9 Graph represetation of Constructive Module Assembly Tree (CMAT).

component, is dependent of a PWB, can be specified by mounting type, and be listed as a group of components with same degree. Finally, each component is subsequently represented as a assemble of most basic "building blocks". Thus, there is another way to interpret the term MGPs by using CMAT. The entities, at most bottom level of *CMAT*, are the MGPs. Each MGP has to be referred by the name of both itself and its parent. Without looking up its parent, it is ambiguous to point a solder joint to a TSOP, since it may be used for J-lead, or for gull-lead. The CMAT shows a generic method to decompose a complex electrical product into a few basic categories of building blocks. The

assembly process of a mechanical model can be followed as the reverse of the direction for decomposition. From pure geometric points of view, the CMAT can be treated as a CSG tree with only "UNION" operations at "parent" nodes.

The name of a MGP, combined with the component type of its parent, is used to link with a looking-up table. The table includes all the definitions of MGPs. It functions like a hash table, which hash a component part to a pre-defined MGP library. Each MPG templet, in the library, has to pre-defined and tested before saved into the library. The parametric approach of creating the MGPs are explained in Chapter 7, Parametric modeling of MGPs. In next section, construction and unitization of a G_{CMAT} will be explained in detail.

6.4 CMAT Construction

The most critical part of constructing a CMAT is to appropriately maintain geometry decomposition information, so that such information may be well retrieved to assemble a model by CMAT. Construction of a CMAT involves four steps: 1) geometric decomposition; 2) representation decomposed parts in G_{CMAT}; 3)generation of data files for describing part geometry and constructing relation; 4)creation of hash table. Since steps 1 and 2, (representation of CMAT) have been covered in the previous section, only a few key issues in steps 3 and 4 are further explained in following.

6.4.1 Module to Module Relationship

The relationship of decomposed parts at each level decomposition have to be thoroughly and precisely described in digital format. Failure of recording any boolean or decomposition information could result in program abortion during the model assembly process. Three record files, for each level of decomposition, may be employed to maintain the relationship information among the decomposed modules. It is easy to observe

that the characteristics of module relationship, at each level of decomposition, could be very different.

1st-level: system to board relation. G_{CMAT}'s root node is always defined as the entire product, and its dependents generally are PWBs, which are slided into slots mounted on a system. Thus, the relationship of PWBs may be sufficiently defined by their physical location and orientation.

2nd level: component-to-component (C-to-C) and component-to-board (C-to-B) relationship have to be defined. Component-to-component relation is the relative location among all components in a board, such as component A is on left of B, and B is on top of C. C-to-C relations may also defined as a directed graph, whose edges represent location relationship of the vertex it attached. The graph may be defined locally, which describe the relative location by looking any two neighboring components. Topological sort may then applied to sort and connect entire nodes in each direction. C-to-B relations are the informations of components mounting types. The shape of physical connection is the primary interest. It will determine a FE meshing method for connecting MGPs, such as by solder joint, or by encapsulant.

3rd level: MGP to MGP relation. The description of information, which associated with decomposition of a component into modularized generic primitives (MGPs), has to be specified. This may seem to be a very complicated step in the third levels, since each component may have different MGPs, and each MGP may have different geometric shapes. However, one MGP may not be attached to all other MGPs. The attachment allowances of a MGP have been defined at the time of creation. Thus, a link-list can be used to preserve the relationship information of MGPs.

6.4.2 Input Data Files

Assembly of a product model implies that a FE thermo-mechanical model of the product will be built by using MGPs. That is, the FE model is “fabricated” by reusing

pre-defined building blocks, instead of creating a new model from scratch. The programming structure for assembly of a mechanical model is showed in Figure 6.10. The required input files, for a product with one circuit board, can be listed as:

1. **Component list.** There are three files for component list. At different level, the term of component refers to different contents. Components are PWBs on 1st level, electrical parts on 2nd level, and MGPs on 3rd level. In the component list file for first level, the location and orientation of each decomposed PWB have to be tagged in data file. On 2nd level, the name of components have to indicate its type and its number. For example, TSOP_GULL(1) indicates that it is a first TSOP with gull lead. There may be more TSOPs on a board, so that they may be listed as TSOP_GULL(2), etc. In addition, the location of each component has to be specified in same file. The location of a component is defined as 2D (x,y) coordinate, where (x,y) is its geometry center projected onto the board. The origin of cartesian system is the bottom-left corner of a board. On 3rd level, besides a MGP link-list, the data of location (x,y,z) and orientation (degree) have to be included for each MGP. Furthermore, each MGP has to be tagged with the component identification of its parent.
2. **Description of geometry for MGPs.** This file, which describes the geometry of TSOP(QFP) components, may be separated into two files. First one is to describe the configuration of a component, such as SIDE_OF_LEAD, NO_LEAD_ON_X, NO_LEAD_ON_Y, PITCH, etc. Second one is for geometry description of each module, such as lead geometry, solder joint geometry, package body. Detailed request geometry for each component and module can be found in chapter 7, parametric modeling of MGP.
3. **Mesh control data.** Though the mesh control information may be completely built-in, it can be implemented only half automatically at this stage. It may be implemented as a fully automatic process, by link a requested type of analysis and input

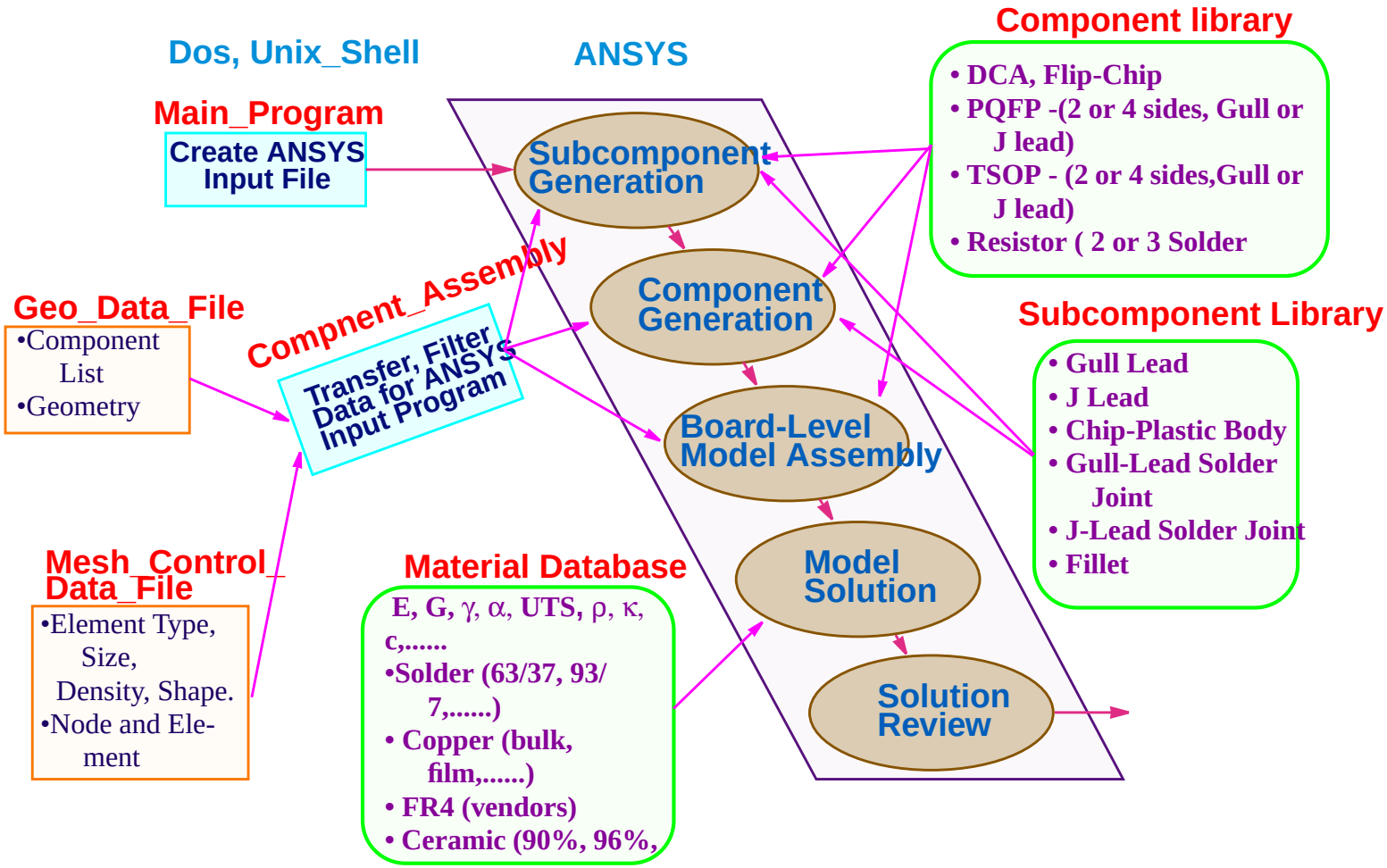


Figure 6.10 Program structure for a mechanical model assembly.

of boundary loads. The data needed for mesh control includes line-division, element size, element-size-ratio, number of element. It may vary in different module, based on the demand of mesh refinement.

4. **Materials.** It is advantageous to let designer only specify the name of materials used in product. Because a product designer may not know what, or how to describe, the material properties in right numerical data format used for mechanical design and analysis. However, this advantageous may lead to ambiguity. One name may correspond to different materials, and same material may have more than two name. "Ceramic" materials have different ceramic alloys. one type of ceramic alloy may have different purity. "Epoxy" may also be called "FP4510". Even same material may have bulk or film format. They all have different material properties. It is assumed, in the scope of this thesis work, the name of material combined with its technical name, identify a unique material. In future, a selection list, as part of user interface, may be provided to identify a correct material.
5. **Main program**. Main program is the program initialize ANSYS software, which is the platform environment for thesis study. It defines the configuration parameters and starting modules. Desired analysis type and loading conditions currently have to be defined in this file.

6.4.3 Hash Table

As mentioned in the previous sections, only the names of MGPs are handled in CMAT. Whenever a MGP is revoked, a link will applied to its template definition. This link is manipulated by a dictionary. A hash table is an effective data structure for implementing dictionaries. A hash table is a generalization of the simple notion of an ordinary array. Direct addressing is applied in the hash table. Direct addressing is a simple technique that works well when the number of keys is small, and no records have same keys. The keys are the attribute variables to be sorted, and the records consists of template defi-

nition of MGPs in a library (or a file). To connect the links of CMAT to defined MGP templates, a direct-address hash table T is created. In the table, each position, or slot, contains a key, which links a MGP in CMAT to its definition in the library. Figure 6.11 illustrates the approach. Slot of Gull_lead points to an record (satellite data) with key gull_lead.

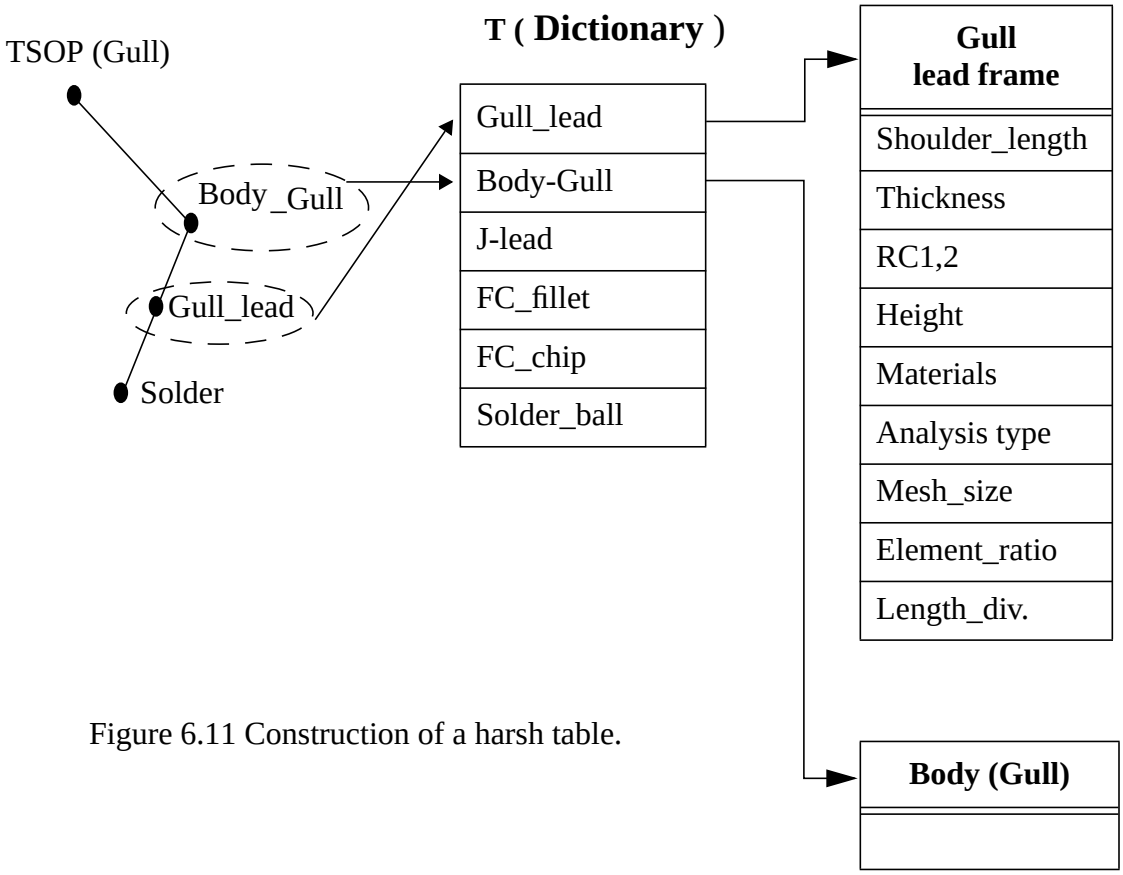


Figure 6.11 Construction of a harsh table.

6.5 CMAT Unitization

Creation of a FE product model, by modularized approach, is a sequence of oper-

ations of SELECTIONs and UNIONs of MGPs. The operations of SELECTION are determined by the leaves nodes on G_{CMAT}, and UNIONs are by the internal nodes. Given a G_{CMAT} for a product, determination of the sequence is the key step for model creation.

In order to obtain a operation order list, a search algorithm is formed. (The assembly procedure is shown on Figure.) It is started from the root of G_{CMAT}, followed by Depth-First-Search (DFS). The strategy followed by depth-first search, as its name implies, to search the deepest part, in CMAT graph, whenever possible. A DFS degrees, represented as levels of decomposition. A DFS are explored out of the most recently discovered vertex *v*, represented for a subcomponent, that still has unexplored edges leaving it. When all of the v's edges have been explored, the search backtracks to explored edges leaving the vertex from which *v* was discovered. This process continues until all the vertices, that are reachable from the root source vertex, are discovered. A DFS therefore gives an order for assembly operations.

Given a G_{CMAT} of a product, vertices are colored during the search to indicated their state. Each vertex is initially white, is then grayed when it is discovered in the search, and finally, is blackened when it is finished. That is, its adjacency list has been examined completely. This technique guarantees that each vertex ends up in exactly one depth-first path. DSF also timestamps each vertex. Each *v* has two timestamps: the first timestamp *d[v]* record when *v* is discovered (grayed), and the second timestamp *f[v]* records when the search finishes examining *v*'s adjacency list (blackened). For every vertex *u*,

$d[u]<f[u]$.

The timestamps are helpful in defining the ordering list for assembly of a model.

The data structure, in C programming, of a node for G_{CMAT} may be structured as in Figure 6.12. The following pseudocode is the basic depth-first-search algorithm for a G_{CMAT}. The input graph of G_{CMAT} is assumed to be in a directed graph, represented by link list. The variable *time* is used for timesamping. *p[u]* represent the degree of a vertex. The significance of degree is that it represents the level of decomposition. Line 1-3 paint all vertices white, and initialize all π fields to NIL. Line 4-5 reset the global *time* and *degree* counter. Line 5 let the starting node be the root node. Line 6 - 7 check the color of root node, if it is white, visit it using DFS-visit. When DFS returns, every vertex has been assigned a degree counter π[*u*], a discover time *d*[*u*], and a finishing time *f*[*u*].

```
typedef struct node {
char *name;
int number;
struct node left;
struct node right;
struct node parent;
} CMAT;
CMAT G;
```

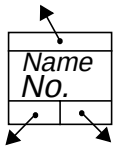


Figure 6.12 Data type construction in C

.

DFS(G_{CMAT})

1. ***for*** each vertex $u \leftarrow V[G]$ ❁ variables initialization.
2. ***do*** *color*[*u*] ← white
3. π[u] ← NIL
4. *time* ← 0
5. *degree* ← 0
5. *u*←root ❁ Let root node be the starting point.
6. **if** *color*[*u*] = white
7. **then** DFS-Visit(*u*)

DFS-Visit (*u*)

1. *color*[*u*] ← GRAY ❁ White vertex u has just been discovered.
2. *d*[*u*] ← time
3. *time* ← *time* + 1
4. **for** each $v \in Adj[u]$ ❁ Explore edge (u,v)
5. **do if** *color*[*v*->right] = white
6. **then** π[*u*] ← *degree*
7. *degree* ← *degree* + 1
8. DFS-Visit (*v*)
9. **else if** *color*[*v*->left] = white
10. π[*u*] ← degree
11. DFS-Visit (*v*)
12. *color*[*u*]← black
13. *f*[u]← *time*
14. *time* ← *time* + 1

In each call DFS-Visit (u), vertex u is initially white. Line 1 paints u gray, and line 2 records the discover time d[u], and line 3 increment global time variable by one. Line 5 - 11 examine each vertex adjacent to u and recursively visit v. For each v, if its right child is white, it implies more decomposition exists. Degree is incremented by one. otherwise, just discovered vertex v has same parent as u, and p[u] remain the same. Finally, after every edge leaving u has explored, line 12 - 14 paint u black and record the finishing time in f[u].

Figure 6.13 illustrates the progress of DFS on a G_{CMAT}. For simplicity, letter a to g have been used to denote real names of components. The denotations are list as follow:

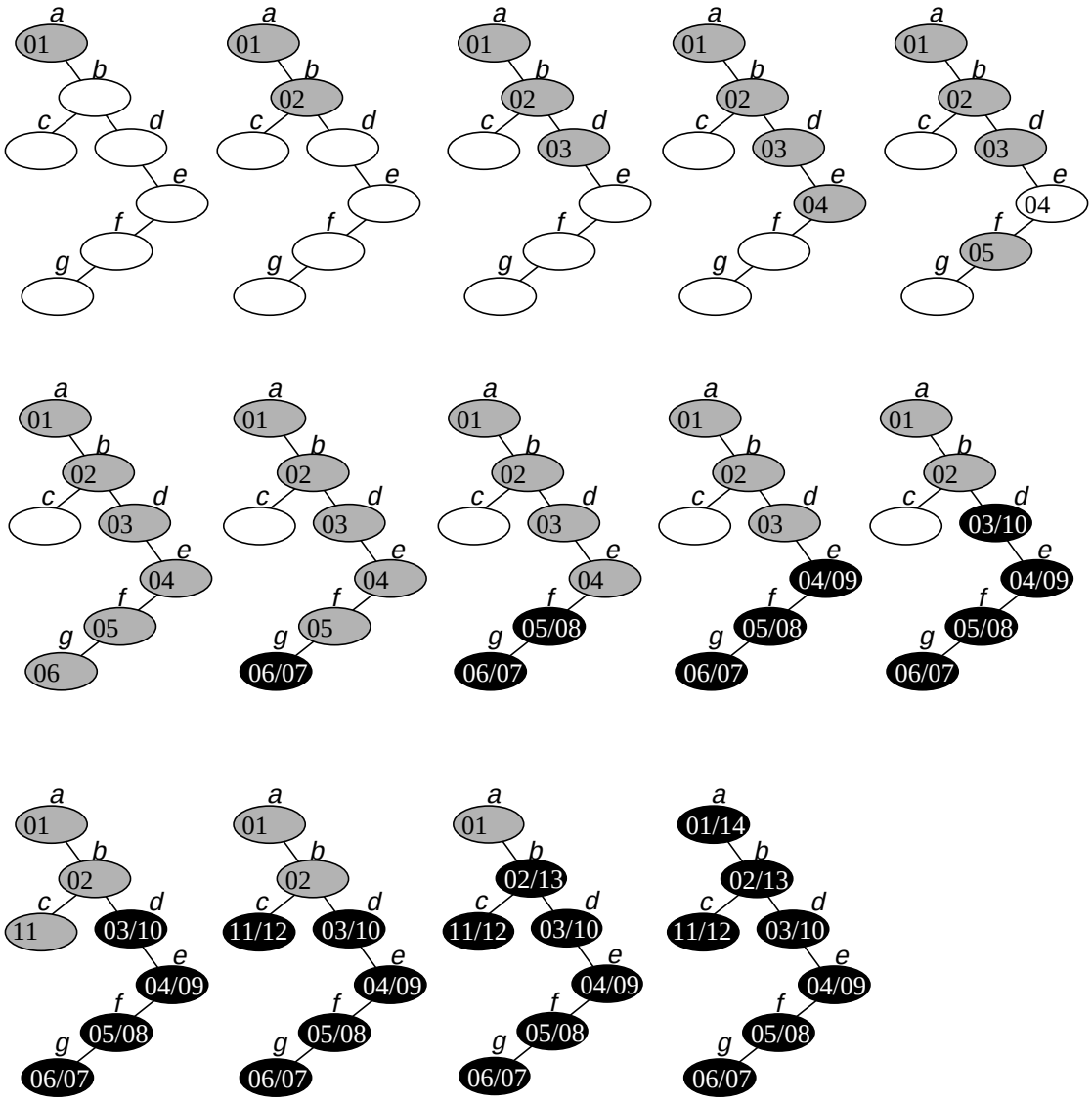


Figure 6.13 Exploration of a G_{CMAT} by DSF algorithm.

a - Card A product with 2 PWBs

b - PWB-01 A board has one component (TSOP)

c - PWB-02 A board has zero component

d - Component-01 The component has three MGPs

e - MGP-01 Plastic body

f - MGP-02 Gull-lead

g - MGP-03 Solder joint of Gull-lead

As seen on Figure 6.13, grey painting started from vertex a, continuously explore deeper vertex until to the leaf vertex e-g (MGPs). Black painting backtrack finding path to d (component), which is the parent of MGPs, and then back to b (PWB-01), which is the parent of the component. Having finishing black painting b (PWB-01), it start to explore c (PWB-02), before back to vertex a. After completely check all the children of vertex a, it goes back to its original place.

A mention before, *p[u]* represent the decomposed level for parts modules. Different level of parts may be clearly checked by *p[u]* variable. In this example, vertex nodes, sorted by p[u], are list as following.

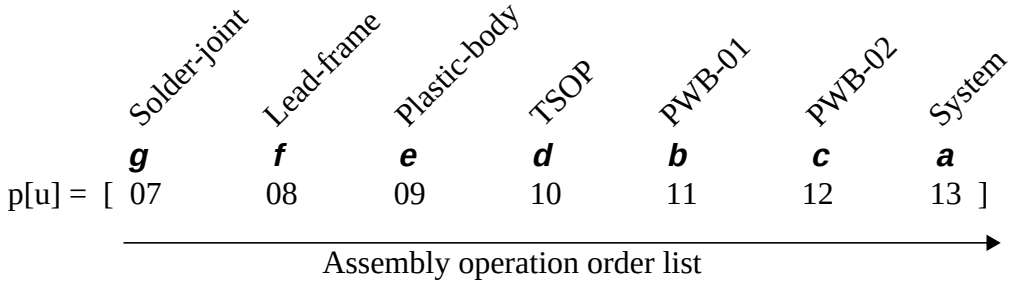
p[u] = 0 : a Product level

p[u] = 1 : b, c Board level

p[u] = 2 : d Component level

p[u] = 3 : e, f, g MGP level.

The discovery time d[u] and finishing time f[u] are used to generate the sequence list of assembly operations. The sequence list can be obtained by sorting all vertices by finishing time f[u], started with vertex with minimum number. Discovery time d[u] is not directly used in assisting creating the sequence list, but it is used to check Parenthesis rule being complied. In the example shown above, the sequence list is as follow:



6.6 Modularized FE Modeling

Another advantage of modularized modeling method is that an analysis model is created simultaneously with geometric model. This aspect is called modularized finite element modeling. The element mesh, associated with element type, is selected according to the analysis type requested in advance.

As mentioned before, creation of an analysis ready FE model is more difficult the than pure geometric model. Geometric modeling of a component, or a product, can be done without much engineering thought. However, without the concern of engineering analysis at the stage of geometric modeling, generated geometric models could be hardly used for thermomechanical analysis. Consequently, a separate geometric model has to be created again for the purpose of analysis. In order to overcome this obstacle, the concerns of generating an appropriate geometry for analysis is built into the MGPs. It is for this reason that requires MGP has to satisfy rule 3 and 4, which are defined in section 6.2.

In geometric modeling, the build-up of an element mesh of MGPs has to start from scratch, along with the creation of the geometric model. Since each MPG is different in its geometric shape, the method used to mesh also varies case by case. Regardless of the mesh creation, they all have to satisfy three conditions:

- Element compatibility condition;
- Rigid body motion constraint;
- Flexibility of nodes and elements modification.

The first condition is must be satisfied by theory of the FEA approach. Most finite element methods are based on displacement rather than stress. Thus, each element invokes a displacement field that is continuous and single valued. More precisely, elements have to be compatible at nodes to the extent of node degree of freedom (d.o.f) they share. For example, if an adjacent beam element meets a node where they share

only translation d.o.f, a hinge like connection is created. One exception is that compatibility may or may NOT be satisfied across the interelement boundary.[cook] Generally speaking, in using a commercial FEA package, specific attention must be paid on not attaching nodes to a line and not attaching two incompatible nodes in same location without other constrains.

The second condition actually requires that equilibrium of nodal forces on moments are satisfied. The structural equations

$[K]\{D\} - \{R\} = \{0\}$

are nodal equilibrium equations, where $[K]$ is stiffness matrix, $\{D\}$ is displacement vector, and $\{R\}$ is loading vector. Therefore, the solution vector $\{D\}$ is such that nodal forces and moments have a zero resultant at every node. However, equilibrium condition is usually not satisfied across interelement boundaries. This rule requires, when generate a FE model, nodes of an element have to be either constrained by other elements or by external loading forces. Positive pivotal errors or warnings are generally caused by not enough constrains, that allow either rigid body translation or rigid body rotation.

The third condition is required by solution convergence and global/local analysis. By providing the flexibility of changing element type and density, a designer may change element density to confirm convergence. The mesh generation is based on defined parameters. In other words, a MGP is defined as a master model. It can be reused as geometry changes. This parametric feature will discussed in chapter 7. The flexibility of meshing may also provide the capability of global/local analysis, as this MGP may isolated from other, and remeshed in more fine element for detail analysis.

It is worthwhile to point out that finite element is an approximation method. There is no clear line to draw between wrong or right on how to model a structural problem. A modeling method can be either warranted by previous confirmed similar problems, or can be compared to experimental test. In an exact solution, according to

the theory of elasticity, every differential element of a continuum is in static equilibrium, and compatibility prevails everywhere. An approximate finite element solution does not fulfill these requirements in every sense.

In order to fulfill these three conditions, the possible neighboring components, that a MGP can be attached to, have to be defined in advance. As a result, this will affect the mesh patterns of a MGP. If a MGP could attach to any possible components, or substrates, it will be impossible to set a general modeling method to satisfy these conditions. Fortunately, a MGP, in electronic application, is generally can only be attached to limited components. For example, a gull shape leadframe may only be attached to a cubic body and substrate through a solder joint, a solder joint in Flip-chip applications only be attached to top chip and bottom substrate.

Given the components that a MGP can be attached to, a meshed pattern can be generated and tested. The pattern selected for mesh can be determined by the common geometry joints. Attached components may only be shared by common line connection, common surface connection, or line to surface connection.

Before the illustrate the detail algorithms for each case, the general meshing concepts are clarified. Regardless the dimension of a object, mesh always starts from points, to lines, surface, and finally to solid. In another words, the mesh of higher level of geometry is based on the meshed pattern of lower geometry, e.g. if the meshing pattern of the lines of a rectangle have been determined, the mesh of the area will based on the line pattern, starting from line perimeter to inside. So, if two lines, belong to two areas, are same in dimension, and the mesh pattern of the lines are same, no matter what methods used to mesh these two areas, these two areas can always be joined by the two lines. The compatibility condition can be automatically satisfied. More general algorithms are list as the following codes. It is assumed that the MGPs are formatted as a link list.

CASE 1. Line-to-line. In this case, it is assumed that any two MGPs only share

common lines. The algorithm may descried as the follows:

COMMON_LINE (MGP_LIST)

1. N ← No. of MGPs in MGP_LIST
2. do i ← 1 to N-1
3. do j ← i+1 to N
4. for each $La \in MGP_i$ and $Lb \in MGP_j$
5. if $La \cap Lb \neq \varnothing$ and $La \neq Lb$
6. then $Lc \cap Ld = Lb$ and $Ld \cap Le = La$

   and $Lc = Ld$ be common line
7. $MGP_i \leftarrow Ld \cap Le = La$ Replace Lb by Lc and Ld
8. $MGP_j \leftarrow Lc \cap Ld = Lb$
9. MESH_INTERIOR(MGP_LIST)
10. Return (1)

MESH_INTERIOR(MGP_LIST)

1. for each MGP_i in MGP_LIST
2. do n_i ← Element divisions on L_i (ni=Length(Li)/di, di = element size)
3. LESIZE, L_i, n_i, ratio
4. If MGP_i is Surface
5. then AREA_MESH(MGP*i*)
6. elseif VOLUME_MESH(MGP_i)
7. Return (1)

In COMMON_LINE part, the input MGPs are assumed in a link-list format. Line 1 find the number of MGPs in the link-list. Line 2 to line 8 check every two MGPs in the MP_LIST, that may have common lines. If $La \cap Lb = \varnothing$, where a and b

denote two different lines belong to two MGPs, line a and b have common shared line. If $La \neq Lb$, then split Lb into Lc, and Ld and La into Ld and Le, so that Lc = Ld, and $Lc \cap Ld = Lb$ and $Ld \cap Le = La$. Line 8-9 update the MGPs whose lines have been split. Thus, common lines are strictly the same, and may be merged together later. Line 9 calls subroutine MESH_INTERIOR, which meshes each MGPs in the MGP_LIST.

In MESH_INTERIOR, the algorithm starts with meshing common lines that have been found in MESH_LINE. Line 2 defines the mesh criteria for the common line L_i. the variable n_i denotes the element divisions on Li. It may also be converted from specified element size, denoted as di, by ni = Length(Li)/di. Line 3 executes the common that divides the Li into ni divisions with a specified ratio. If MGPi is a surface module, then use common method to mesh MGPi, otherwise, use volume method to mesh MGPi. The area or volume meshing methods are defined by parameters, which will be discussed in next chapter.

CASE 2. Surface-to-Surface. If two MGPs have shared common surfaces, or even part of a surface, the algorithm may be as follows:

COMMON_SURFACE(MGP_LIST)

1. N ← No. of MGPs in MGP_LIST
2. do i ← 1 to N-1
3. do j ← i+1 to N
4. for each $Sa \in MGP_i$ and $Sb \in MGP_i$
5. if $Sa \cap Sb \neq \varnothing$
6. then $Sc \cap Sd = Sa$ and $Sd \cap Se = Sb$ and $Sc = Sd$
7. $MGP_i \leftarrow Sc \cap Sd = Sa$ Replace Sb by Sc and Sd
8. $MGP_j \leftarrow Sd \cap Se = Sb$

9. COMMON_LINE(MGP_LIST)

10. return (1)

Similar to the case of Line-to-Line, COMMON_SURFACE first checks each pair of MGPs that may have common surface. If so and they are not the same, Line 4 to Line 6 split the surface, so that they have a common surface. The implication of common areas is that the MGPs have only common lines, which define the common surface. Thus, the surface-to-surface problem is converted to line-to-line problem. Line 9 calls COMMON_LINE function to continue solve line-to-line problem.

CASE 3. Line-to-surface. This case may be solved by split the surface which the line is lying on, so that they can have common lines. COMMON_LINE function can then be applied. Since the algorithm for this case is simple and similar to surface-to-surface, it is skipped.

6.7 Substructure (Superelement)

This section is intended to clarify the difference between the modularized finite element method and the substructure technique.

Substructuring is a finite element technique that allows you to create a FE model from fine to coarse. In this procedure, it simply condenses a group of elements. The remaining nodes are called master degrees of freedom, and this new “big” element is called a super- element. In this super-element, all the nodes, except those of lead connected to board, are condensed. The density of master degree of freedom will be adjusted by its defining parameters. The calculation will only give the solution to the nodes of interest, while the effects of the whole package behavior are still included. Generally, a substructure procedure involves three passes: generation pass, use pass, and expansion pass. No further approximation is taken for this technique. A limitation is that it is only valid for linear problems. An assembled mechanical component may be

used as a super- element in solution pass, such as group entire model of a leadframe as a superelement.

Though the modularized model can be used as a superelement in solution pass, it significantly differs from the super element in the following aspects:

Geometry shape. The geometry shape of a superelement can not be changed, but a MGP can. As described in previous paragraph, a superelement is only corresponding to a specific geometry shape, because the stiffness matrix is function of geometric interpreting function. Once the geometry is changed, the superelement is no longer valid, the meshing procedure and selection of master degree of freedom have to re-start from scratch. But the MGP has the flexibility of change mesh automatically according to the default value, or new requested criteria, since the mesh is independent of a particular shape of geometry, but function of the topology of the geometry. So different geometry, in same topology, require different superelements, but only need one MGP FE model.

Element type and material properties. The element type used to form superelement can not be changed after the definition. Since the stiffness unit to assembly superelement stiffness matrix is based on a pre-selected element type, the change of element type, e.g., from 4 node element to 8 node, will result in redefine a new superelement. In modularized FE modeling, the element type is a link from a meshed model in an element library, the change of an element type will only require modify the linkage to a new element, and leave others unchanged. Same reason is applied to the material properties.

6.8 Example of Modularized representation

This section gives an example of modularized FE modeling of a BGA structure. It will show the flexibility of a BGA FE model.

Ball Grid Array (BGA) interconnection is a second-level surface mount electronic packaging technology. A ceramic module containing one or more chips is attached to a circuit card (FR-4) by means of an array of non-homogeneous solder balls. These connections consist of a high temperature melting solder (90Pb/10Sn) sphere attached to the module and card with eutectic solder fillets. The solder structure offer both electrical connection and mechanical support. They accommodate the bulk of the strain generated during the power cycling and the manufacturing process.

In order to provide a more compliant joint for better reliability, the structure of a BGA connection should be well designed and its behavior should be well understood. The parts needed to create a BGA interconnection are:

- Chip(0-level) substrate
- upper solder pad for eutectic solder
- upper eutectic solder connection
- Non-eutectic solder ball
- lower eutectic solder connection
- lower solder pad for eutectic solder
- Board (1st-level) substrate

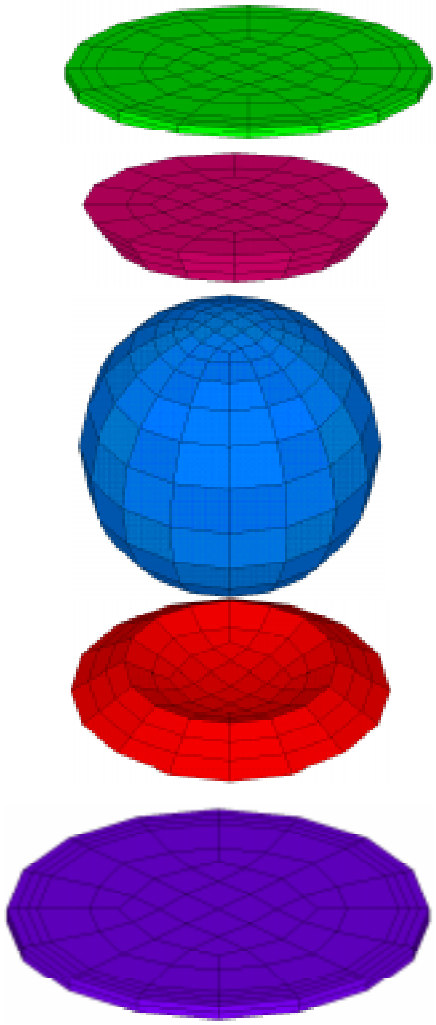


Figure 6.14 Modularized parts for a BGA modeling

These seven parts are defined (Figure 6.14) and stored in a library for a BGA model assembly. Each part of a geometry shape and mesh grid are flexibly controlled by build-in parameters. More detail of using parametric modeling method may be found in next chapter. For example, the solder ball may

be stretched vertically or horizontally to form a taller or shorter elliptical ball. The parameters used for the upper eutectic solder connection and non-eutectic ball are listed below:

1. Upper eutectic solder connection: base radius, cover-angle, volume, fillet profile, material ID to material properties data-base, algebra relation to eutectic ball, mesh line division, mesh density ratio, element type, element size, and number of coupled nodes.

2. Non-eutectic solder ball: ball width, ball height, ball profile control point, cover angle and volume of upper and lower eutectic solder, mesh line divisions on each direction, mesh grid ratio, element size, element type, material ID, algebra relation to upper and lower eutectic solder, and node coupling points.

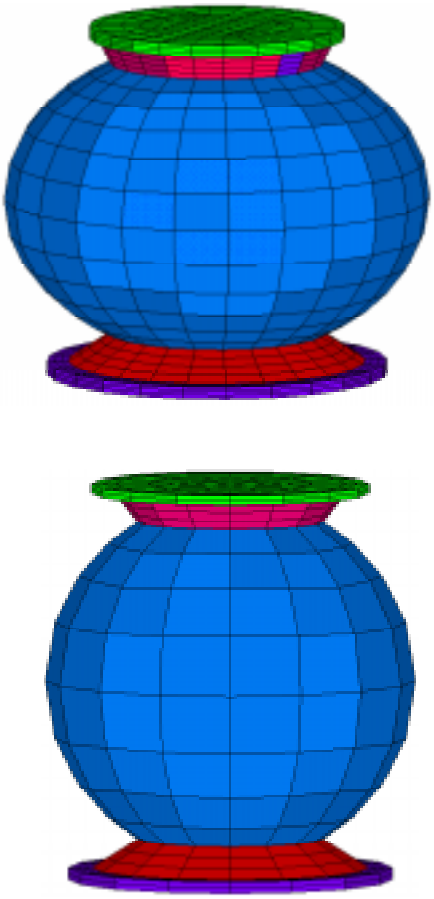


Figure 6.15 Two BGA FE models based on one modularized Model.

The modularized parts in a library are virtual models without real geometry data for the parameters. Some parameters are input directly, while others are depend on the parameter values of neighboring parts. Construction of two BGA connections with different configuration is shown on Figure 6.15. In each construction process, the parts are called one at time to assemble a BGA connection. The geometry relations and element connection are maintained by a graph tree. All the parts of two BGAs have different configurations and mesh densities. The left side BGA has a shorter and wider

ball with fine mesh, and right one is a perfect sphere with coarse mesh. The configuration and mesh distribution for each part of a BGA model may be modified even after the model creation. Other connected parts will be modified automatically and simultaneously, since they all controlled by the graph tree.

Chapter 7

Parametric Modeling Approach

The main idea of the parametric modeling approach is to create or define a model template by parameters and its forming rules, instead of a specific model. The template can be used to generate an actual analysis model by populating data into the parameters of a template. A template serves as a master model mock-up, and is used for one-to-many modeling activities.

The development of a parametric modeling approach, in this thesis, is explained in the following sections. Section 7.1 introduces the feature-based parametric representation for geometry and FE modeling, followed by how to parametrically build a MGP model according to its forming rules and parameters, which is described in Section 7.2. A mechanical component library and material database are outlined, in Section 7.3. In Section 7.4, the general description of a global/local analysis is presented as an extended capability of parametric modeling.

7.1 Feature-Based Parametric Representation

The parametric modeling approach has several advantages, which include flexibility, interchangeability, and transportability. Flexibility of a model implies that the model may be modified easily to create a new one in the initial design process, but also be able to answer “what if” questions at the design analysis process. Interchangeability

refers to the compatibility of unitizing a model, which may be modified later, if necessary. Since there is no data, or number, employed in the procedure of defining a model template, the process of an actural model creation and a model definition are separated. Model hierarch and abstraction can be easily achieved. Internal changes of a model template and model encapsulation can be independently implemented without altering the manipulating methods and techniques for the model. Transportability suggests that the developed model templates be independent of either software platforms or design applications. The development of a template involves, only, the definitions of forming rules and parameters used for describing these rules. The rules are created by design applications, not the software actually implementing it. Thus, the model defined by a model template, in a software environment, can be readily transferred to another environment.

7.1.1 Topdown and bottomup geometric modeling approach

Before creating a finite element mesh for a geometric model, a geometric model must be generated. There are two general approaches that can be used for the generation of a geometry model. They are called topdown modeling and bottomup modeling. Topdown modeling is to create a geometry model by using solid geometry primitives provided in a design environment, followed by boolean operations, such as addition and intersection, to obtain a desired shape and geometry outline. Bottomup is to create a geometry model from definition of points, then to lines, surfaces, and solids. These two modeling methods have their own advantages and disadvantages. It is impractical to determine that one approach is more superior than another without an application.

Advantages and disadvantages for topdown modeling:

- It is fast to create a 3D geometry model, when the model is similar to an existing primitive in a system.
- It is generally more appropriate for a large, or complex model, especially 3-D

model with solid volumes.

•Since the users only need to control geometry primitives, it allow him to work with a relatively small number of data item. Thus, the management of data structure is easy to handle.

•By using a 3D geometry primitive object, the attributes, such as surfaces, lines and points, associated with this object, can be easily selected or accessed. It will allow the geometry operation, such as rotation, be performed on the entire object, instead of specifying more detailed operations on attributes.

•It supports different primitive area and volume, such as polygonal areas and cylindrical volumes), and boolean operations, such as intersection and substruction, for constructing a geometry model.

•It may be required for adaptive FE meshing.

•Geometry modification is performed on 3D primitive object.

However,

•It generally requires large amounts of CPU time.

•For some small and simple models, it may be more cumbersome, and requiring more data entries than direct generation.

•It sometimes can be failed under certain circumstances, such as degeneracy.

Advantages and disadvantages for bottom-up modeling:

•It is convenient for small or simple models.

•It provides users with complete control over the geometry and numbering of every attributes, from points to solids, and from nodes to elements.

However,

•It is usually time consuming. The volume of data that must be worked with can be overwhelming.

•Sometimes, it may not be used for adaptive meshing.

•It is more prone to committing errors.

7.1.2 Parametric Representation of Geometry

The parametric modeling method used for points, lines, and surface is summarized as follows.

Points: Thought there are a numerous ways of defining a point, a few common and practical methods, that allow parametrically define a point *P*, are listed in the following:

a. *P(x, y, z)* in a specified coordinate system, may be cartesian, or cylindrical, or spherical. Coordinates *x, y,* and *z*, may be parameter variables used for the points, or may be determined by other functions.
b. It may determined by intersection of two lines.
c. It may be defined by offsetting (Δx, Δy, Δz), with relative to a previous defined pointed point.
d. It is defined by being offset from a previous point in a direction relative to a existing line.
e. It is defined at equal intervals between two points or along a line or curve.

Line: The lines, in the scope of this thesis, are limited to straight lines only. They can be defined and constructed in the following ways:

a. It can be constructed by two existing points.
b. It can de defined by a direction vector through a existing point. The direction vector may be specified as $(\hat{x}, \hat{y}, \hat{z})$.
c. It can be obtained by parallel and offset relative to a previous coplanar line.
d. One line may be a result of bisecting, splitting, or concatenation operation.
e. It may be a line that define a surface primitive. For example, it may be one of the four lines constructed a rectangle. The parameters, associated with this line, would be line number, two corner points on the line.
f. It may be a line that define a solid geometry primitive, such as a line in a tetrahe-

dron, or a cubic box.

Surface: Similar as line, the surfaces are limited to planar areas only. The parametric definitions of non-planar surfaces are dependent on their particular characteristics. Each type of non-planar surfaces can be described exclusively within its class, such as cylindrical surface and spherical surface. Here, a plane, which is a planar primitive, can be constructed in the following ways:

a. It can be defined by defining of coefficients of the equation Ax+By+Cz+D=0.
b. A rectangle may be defined by two opposite corner points, or one point and length of each side, or a fixed line segment and a point.
c. A circle, or a arc, can be uniquely determined by any three parameters of origin, radius, starting point (angle), end point (angle), drawing direction, and points on circle lines.
d. A planar primitive may be obtained by offset previous one.
e. It may be part of a solid model.

Since the parameters used for a solid geometry primitive are not likely the same for different applications, the 3D solid geometry primitives have to be classified, before introducing the parameters for each primitive. However, the concept of constructing a solid by parameters are same as surfaces and lines, detailed definitions of parameters for solids are skipped.

7.1.3 Parametric Representation for FE Modeling

As mentioned in previous chapters, a geometric solid model is used to help a designer visualize the design concept, but it can also be used for more comprehensive analysis and prediction. The same geometric model, however, has to be able to perform different design studies. In order to achieve this, not only geometric parameters, but also analysis parameters have to be built into the model template.

For the completion of the model, which can perform a specified FE analysis, the following parameters have to be explicitly defined: element types, element attributes, initial condition, material properties, loading, solution criteria. These information have to be provided in parametric forms, so as to enable flexible changes and reuses. The following items are all necessary attributes that have to be determined for a parametric FE modeling approach.

1. **Element type:** Before an element can be used, the type of an element must be defined. There are six parameters that used to defined the information associated with an particular element. For example, the parametric representation of a 3D 8 node element is shown in Table 7.1.

Table 7.1 Parameters for defining an element type

Attributes	**Data**
Element_name	SOLID45
element_type	structural solid element
element_No	2
Element_node_No.	8
Element_mid_node_option	1[a]
Element_capability	ss,m,t,n**[b]

a. 1 for YES, and 0 for NO.
b.ss for stress-strain, m for modal, t for thermal, n for non-linear

2. **Element features:** The parameters, used for element attributes of each element type, store information for reuse and quick access. Since each element type is different than others, some parameters can be different. The parametric representation of element attributes, for element type SOLID45, are listed in Table 7.2. Parametric representation

of other element type may be obtained in a similar manner.

Table 7.2 Parameters for defining element features.

Attributes	Data
Node_No	i,j,k,l,m,n,o,p[a]
Real_constant	NONE[b]
Material_Type	1,2,3[c]
Material_properties	Ex,Ey,Ey,ALPx,ALPy,ALPz
Analysis_Feature	Pl,Cr, Sw, STRs, LD, LS, BD[d]
Displacement_shape	0,1[e]
Coord_system	0,1[f]

a.From top to bottom in counter-clockwise
b.Not available for this element.
c.1 for linear, 2 for bi-linear, 3 for time dependent.
d.Pl for plastic,.....
e.0 for extra, 1 for suppress extra
f.0 for global, 1 for local

3. **Meshing size or density**: A desired element mesh may be obtained by either specifying element size(Es) or element density(Ed). But element size and density can be used differently. Usually, the element size refers to the edge length of an element, and the element density represents the number of elements to be used for a given bounded space. When using element size as a parameter, minimum or maximum size can be input by a user for an automatic, or half-automatic, meshing operation. But, a meshing solution may not be obtained for the given sizes. Specifying element density parameter is more superior at this point. It almost guarantees a solution, but the aspect ratio of certain elements may not be satisfactory. Parameters of density ratio is usually used, together with an element density parameter, to achieve a better solution.

- **Meshing lines:** A line can be meshed in 4 method: 1) Equally divided a line into L_n line segments, where L_n is the given parameter. Ending point of each line segment will be nodes for an element. 2) Equally divided a line into L_n segments, such that each size of a line segment is close to the length L, where L is denoted to line size and is the given parameter. 3)Divide a line into Ln segments, such that the line segment ratio, which is defined as the line segment at one side to that on other side, is equal to L_{ratio}, where both Ln and L_{ratio} are the given parameters. 4) Similar to 3, but replace Ln by length L.
- **Mesh areas:** Two meshing operations may be applied to an area: free mesh or mapped mesh. In free meshing operation, no special requirement restricts an area. Free meshing can using either mixed element shapes, or else all triangular area elements. Using parameters as element shape commands, such as ESHAPE, to instruct programs to choose the element shapes. Notice that, the free mesh operation is always starting from key points to lines, then to the interior of an area. If the lines has been meshed, the free mesh operation will generate elements based on the pattern of the lines. This actually allow a designer to control the meshing operation. In mapped mesh, it requires that an area has to be regular, that is, it must meet certain special criteria: The area must be bounded by either three to four lines; b) it must has equal numbers of element divisions specified on opposite sides; and c) the number of element divisions must be even if the area is bounded by three lines. It can be seen that the meshing of an area is primarily dependent on the meshing of lines. After the lines of an area have been meshed, the following parameters and control commands, in ANSYS, can be used:
  - ESHAPE,kshape,kstr !control the element shapes
  - LCOMB,nl1,nl2 !combine adjacent lines into one line

- AADD,na1,na2,..... ! add separate areas to create a single area.
- ACCAT,na1,na2 !concatenate multiple areas for mapped meshing

- **Mesh Solids (3D)**: Meshing operations for a 3D solid are similar to meshing an area, that is, the operations are based on existing meshing pattern of the areas that bounded the solid. Similar parameters and meshing control commands may be found in ANSYS. It is very important to realize that the meshing procedure is started with points to lines, then to areas, solids, finally, to FE nodes and elements. Without the check of cross-reference parameters, simply modify a higher level of an entity will cause catastrophic errors.
- **Adaptive mesh:** Adaptive meshing is used when the number of elements, or the quality of existing element pattern, are not good enough to produce an accurate result. The meshing results may be improved by either increasing the number of elements or adding mid node to elements. If increasing the number of elements is preferred, points and lines are used to specify new meshing density. For example, set KYKPS=1 will invoke the ADAPT macro to remesh all selected key points. KYKPS is a default parameter used to control remesh pattern in ADAPT macro. ADAPT is a program macro, that contains a series of commands. Both KYKPS and ADAPT can be modified for a desired remeshing result. If the addition of mid side nodes is chosen, the existing element shape are not changed. Only the shape function, associated with each element, is changed to higher order function. By specifying the parameters in EMID and MODMSH commands in ANSYS, additional mid nodes may be added to existing elements. However, not all element types allow this operations.

4. **Initial boundary condition:** The initial boundary conditions imply only to the initial deformed shape of a product model. Other initial conditions, such as initial

temperature, is specified, as initial loading conditions, in the solution pass. The initial BCs contain the deformed shapes, that maybe observed before or manufacturing process. These information are used to perform sensitivity studies on initial shapes. The parameters used for modeling initial conditions, apparently, will dependent on a particular object model and used geometric primitives. One example would be the initial conditions for a PWB, in Flip-chip on Board analysis. Warped-up or Warp-down are two possible initial parameters to determine the stress value as function of temperatures (figure 7.1). The initial shape of the board may be represented by a curve with RC, instead of by a straight line.

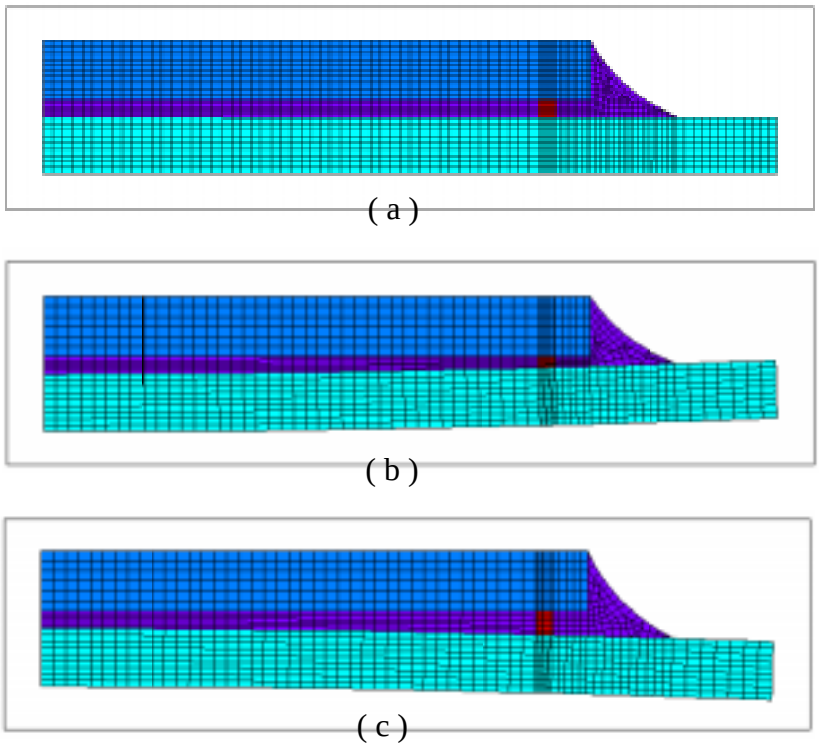


Figure 7.1 . Board initial condition: (a) flat; (b) warped-up; (c) warped-down.

5. **Material Properties:** In general, the values of all material properties have to be

given before the FE model generation. This will cause difficulty for model modification in a repeated analysis, such as in a material sensitivity study. In parametric modeling approach, the material properties are linked with pre-defined parameters, which can be determined, or input from some external resources. By this way, any change of a material properties, in external resource, will be automatically feed back into the model, and leave the original FE model intact.

6. **Initial loading conditions:** The initial loading conditions include all the external loads added on to a model, such as temperature load and bending load. These loads have to be applied to either specific elements, or element nodes. When a model is changed, the loads have to be modified, accordingly. By parametric modeling approach, the value of loads and loads location can be automatically modified with the change of model geometry, and be added to appropriate nodes or elements. For an simple example, a bending moment is applied at one end of a DCA assembly. The initial loading conditions may specified as:

    1. NODE_SELECT, S,LOC, length_form_center_to_edge
    2. D,M,all,value_of_moment

Line 1 select all the nodes at x= length_form_center_to_edge, which is the function of parameters of the initial geometry input. If the length of board is increased, the length_form_center_to_edge will changed with it. In line 2, the D command in ANSYS specify the loads for all selected nodes. The parameter of value_of_moment can be given by user at the time of solution, or it may be assigned from other calculations.

7. **Solutions:** There are three solving methods for a solution procedure. A problem can be solved by load step file method, array parameter method, or multiple solve method. These three methods are written in program macro module with parameters.

The **load step file method** probably is the most convenient method. It involves

writing each load step into a load step file. The format of this method may be written as an macro, and is shown below:

```
1. C**** macro module for load step file method.
2. /SOLU                    !enter solution
3. ........
4. ! Load step 1:
5. SELECT(NSEL),.....       ! select geometry entities, nodes, or elements by
                            parameters
6. D,.....                  ! use load parameters to assign values
7. SF,.....
8. NSUBST,.....             ! load step option
9. KBC,.....
10. .......
11. LSWRITE                 ! writes this load step into a file.
12. !load step 2:
13. ......                   ! similar to load step 1.
```

The array parameter method is mainly for transient or non-linear analyses. This method involves building tables of load versus time array parameters and is explained as following example.

There are three load functions shown above. All these parameters may be defined as arrays. The force has five points, so it needs a 4x1 array; the pressure needs a 6x1 array; and temperature needs a 2x1 array. Notice that all three arrays are one dimensional. The load values are entered in column and the value are entered in column zero. They have to be filled with a monotonically increasing set of numbers. To define the three parameters in ANSYS, *DIM command may be used to define three array parameters force[4x1], pressure[6x1], temperature[2x1]. To apply these loads and obtain the

Force

Time	Value
0.0	100
15.0	200
25.0	200
32.0	350

Pressure

Time	Value
0.0	800
8.0	1200
15.5	1000
20.5	1000
27.0	1500
32.0	1800

Temperature

Time	Value
0.0	350
15.0	200
32.0	75

solution, the following macro module may be used.

```
1.  C**** macro module for array parameter method.
2. *DO,tm,tm_start,tm_end,tm_incr
3. TIME,tm
4. F,272,FY,force(tm)
5. NSEL,.....
6. SF,ALL,PRESS,pressure(tm)
7. NSEL,ALL
8. NSEL,.....
9. BF,.....
10. BF,ALL,TEMP,temp(tm)
11. NSEL,ALL
12. SOLV
13. *ENDDO
```

Without this method, changing the time increment for such a complex load history would be quite cumbersome.

The multiple solve method is the most straight-forward method. It involves

issuing the solve command after each load step is defined. The main disadvantage is that next load step and solution has to be waited after previous one. A typical program stream in a macro module is shown below:

1. C**** macro module for multiple solve method.
2. /SOLU
3. .....
4. !load step 1
5 . SELECT(node),.....
6. D,.....
7. SF,.....
8. solve
9. !load step 2
10. ! similar to load step 1

As seen in these examples, these three method have their own advantages and disadvantage. They may be written in three defined macro module with parameters. A user may simply use one of them by substituting number and values into parameters defined in each module.

7.2 Parametric Representation for MGPs

Modularized generic primitives (MGPs) introduced in Chapter 5, are parametrically modeled for a one-to-many modeling capability. The modeling process involves three steps: description of a MGP geometry variations; definitions of parameters for both geometry and FE modeling; and construction and test of a MGP. In the step of geometry shape definition, the flexibility of a MGP has to be explicitly specified. Though a MGP can be starched to form a new shape, it is yet constrained. The more flexibility of a MGP, the more difficult rules have to be defined for constraints. Consequently, the struc-

ture of a MGP become more complex and difficult to model. The definition of parameters for the geometry and FE modeling are primarily dependent on the needs of MGPs in later design and analysis. The implementation of construction and test for a MGP, in final step, may be vary on different software platforms, but the concepts and procedures remain the same.

Parametric modeling of MGPs are performed after modularized modeling procedure, as introduced in chapter 5. As an extended modeling part for the development of MGPs, used in previous chapters, parametric modeling of DCA and TSOP is shown in the following sections.

7.2.1 Description of geometry variations.

For DCA components, in the scope of the thesis, is limited to die attach onto a FR4 organic substrate only. It is treated as the first level packaging interconnection. The underfill Encapsulant is formed by dispensing epoxy around two side of die, not by injection, so that the fillets of epoxy are appeared on sides. As a preliminary modeling study of a populated board, no solder balls are placed underneath the die. The contribution of warpage from solder balls can be neglected. This is because the silicon is very strong, and it is coupled with FR4 board by epoxy. The variations of die include die size, underfill size, fillet shape, and board thickness. Modeling emphasis of TSOP components are placed on gull and J lead components. The solder joints, which connect the leadframe to board, is assumed to be perfectly aligned with lead frame in global analysis. The lower end of leadframe is assumed to be flat, and parallel with board. Since the leadframes are much more compliant than the package, the stiffness contribution, from the die inside the package, is ignored. The width, thickness and pitch of leadframes are assumed to be same. The variations of gull lead, or J lead components, include package size, leadframe size and shape, solder joint shape, number of leadframes on each side, and board thickness.

7.2.2 Definitions of parameters for both geometry and FEA.

Though the possible geometry variations of these components may be changed, the variations considered in this research work are explained and listed as follows:

For DCA:

parameters:

Locations: x0, y0, z0 *! in global coordinate system.*

Die size: Dl, Dw, Dh *! define length, width, and thickness.*

Undefill: El, Ew, Eh

Fillet size: Fl, R ! *define fillet extension and RC*

Min. space: Cl, Cw *! define the min. clearance for DCA.*

Board thickness: PWB_T

Materials: M_No1, M_No2, M_No3 *! define material one as epoxy, and two for silicon, and three for FR4.*

Line divisions for each geometry attributes: Dl1 for Dl, Dl2 for Dw,.....

Constrains:

!ensure correct fillet size.

Max(Dh+Eh, Fl)+0.3*(Dh+Eh+Fl) < R < 100*(Dh+Eh+Fl)

! total estate area

(Dl+Fl+Cl)x(Dw+Fl+Cw)

! element size of underfill is same as that of die

D_Dl = D_El; D_DW = D_EW

! others

.....

Since specifying either the line division or element size of a line is equivalent, as element size may be obtained by dividing the line length to line division, line division parameters are used to control the mesh generation. The names of parameters for mesh

control, given to each geometry parameter, is defined as adding prefix D_ to the parameter for geometry. Suppose that the die has a length of DL, then the mesh control parameter is D_DL, that is the line is divided into D_DL divisions. By default constraints, the opposite die edge has same length, it is meshed into D_DL divisions as well. The generation of geometry of die is topped of underfill. As the thickness of the underfill increased, the die location is changed correspondingly. Similarly, The total height of the fillet is the summation of both die and undefill thickness. Some constraints are believed to be self-evident, and are not listed above. The actural implementation are encoded in programs, see appendix II

For TOSP with Gull lead:

Parameters:

Lead size: l1, l2, h. r1, r2, w, t, m_no,dl1, dl2, dh, dr1, dr2, dw

! l1 is lead shoulder, l2 is lead base, h is height, r1and r2 are turning curvature; w is width, t is thickness, m_no is material number. all the parameters start with d are line division.

Package: leadside, w, nx, ny, mx, my, sx, sy, thickness, m_no, dw, dmx, dmy, dsx, dsy

! w is lead width; nx and ny is lead number on x and y side; mx and my are leadframe margin offset from package corner on x and y side. sx and sy are separation of leads on x and y side; m_no is the material number for package material.

Solder joint: l2p, l2m, s_h, m_no, ds_h, d_ratio

! *l2p is solder joint extension beyond leadframe, in a direction of away from package; l2m is similar to l2p, but in the direction of into the package. ds_h is the number of number element needed for solder connection, d_ratio is to control the element size ratio.*

FR4 board: x0, y0, z0, rot0, ll, lr, lh, uh, pwb_t, m_no, dll, dlr, dlh, duh, dmx, dmy, dsx, dsy

!x0, y0, z0 is the center location of the component, rot0 is the rotation angle; ll, lr, lh, and uh are the minimum clearance for this component on lower left and right, upper and bottom side; pwb_t is the thickness of the board. dsx and dsy are for element numbers on board, it may not be the same as dsy and dsy in package.

constraints:

!package size

Package length = 2*mx+(nx-1)*(w+sx)+w

Package width = 2*my+(ny-1)*(w+sy)+w

!package location

package z-location = s_h+r1+r2+h

!others

Since some of constrains are self-evident, such as lead width has to be the same as that on package, they are simply skipped. But, there are some important constraints that have to be careful in modeling. They include node-to-element coupling, leadframe offset, lead to solder connections. Since most of the deformation of a TSOP package is on lead frames, there is no need of using lots of elements for modeling the package. The element size, inside the package, is made to be much larger than boundary elements. The displacement compatibility of these elements are enforced by node to node, or node to element coupling constraints. The location of the nodes are dynamically calculated, based on component configuration. Both geometry and FE models of a gull leadframe and its solder connection are created only once. They are duplicated, followed by translation and rotation, to form the attachment in correct locations for an entire lead frame structure. The connection between a solder and a leadframe is very important, and should be cautious in modeling. The compatibility of meshed elements is guaranteed by

setting the line divisions of the solder be the same as that of the lead frame. A double link data or directed data structure is used fulfill this requirement.

To easy the geometry data input for TSOP with gull lead, a window template can be created, as shown in figure 7.2. The programing part of graphics user interface is regarded as an extended research work, and is currently under development.

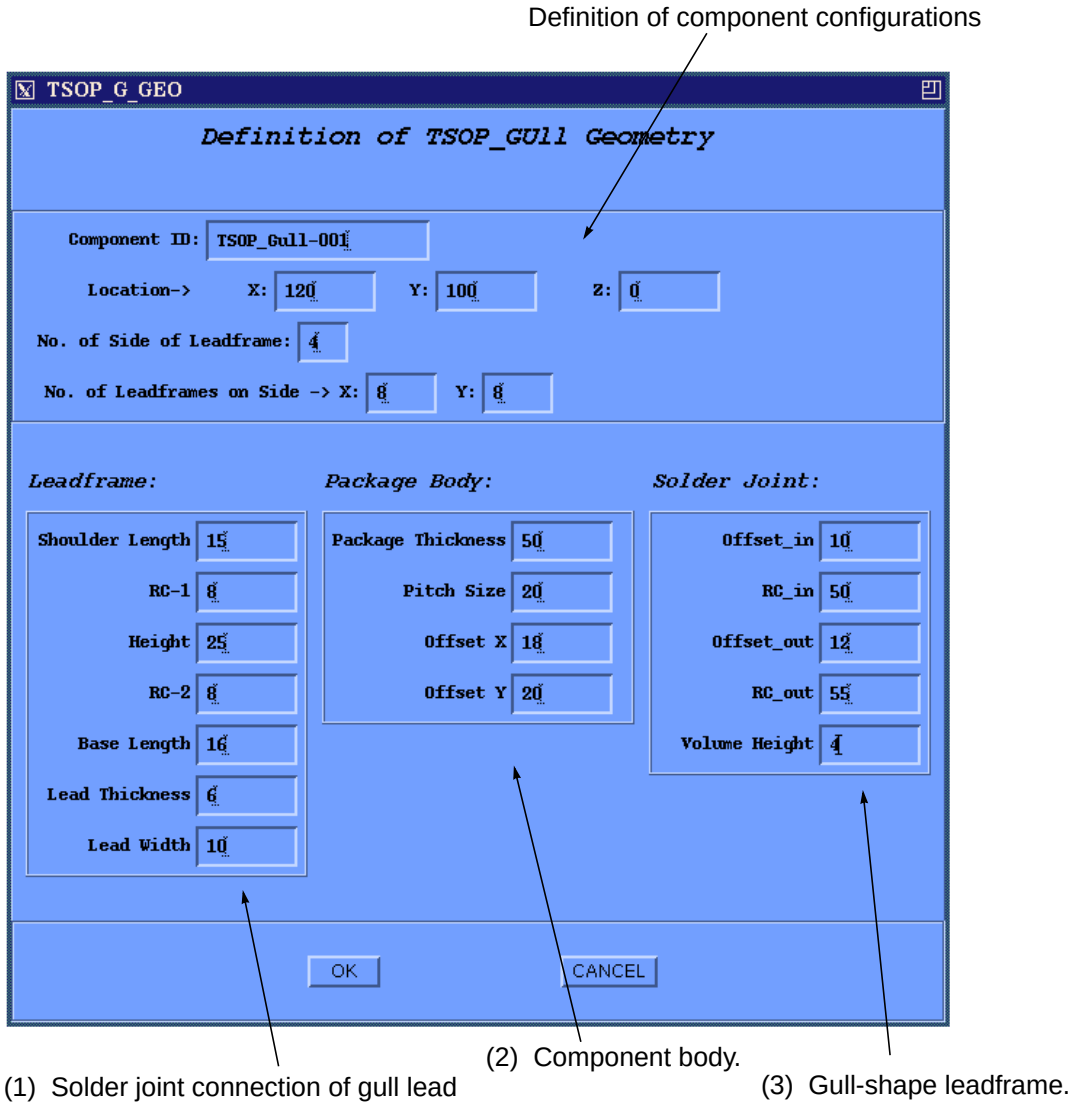


Figure 7.2 Definition of parameters for a TSOP component

Because the TSOP with J leads is similar to that with gull leads, the detail description of parameters for gull lead are not listed.

7.2.3 Construction and test of MGPs.

The construction and test of MGPs are to translate modularized and parametric definitions and methods into programming codes. ANSYS software is used as platform to implement the program. The construction and testing results are explained by examples, which is shown from Figure 7.3 to 7.5.

In Figure 7.3, the MGPs of DCA is created. From Figure (a) to (b), the die thickness is reduced. The fillet on the side is reduced correspondingly, by the constraint rule that the fillet should be the same as die. The number of meshing elements are reduced to maintain the aspect ratio. From Figure (a) to (c), the fillet is modified. The fillet curvature is set to be more concave, that is, the radius of curvature (RC) is smaller. It is noted that the RC is bounded by certain conditions, as mentioned in previous section. This is to prevent excessive element aspect ratio and geometry degeneracy. As seen on the figure, the elements on the fillet corner become more distorted, compared to that in (a). The smaller RC, the worst it will be. From (c) to (d), the die size ratio is changed. A squared die is squeezed down to a slim one. As a result, the DCA estate area is also reduced, but the minimum clearance area around the die are kept the same. The meshing pattern on the board is modified to match the change of die size. Figure (e) gives a perspective view of fillet around die.

Four tested TSOP with gull lead are showed in Figure 7.4. In case (a), a simple two side TSOP is generated first, without solder connections. In case (b), not only lead is stretched larger, and the package becomes thicker, but also the solder joints are attached to bottoms of lead frames. As meshing pattern of solder is coupled with that of leadframe, the elements compatibility is automatically enforced, when solder joints being placed in correct positions. In case (c), the number of lead frame on both side is

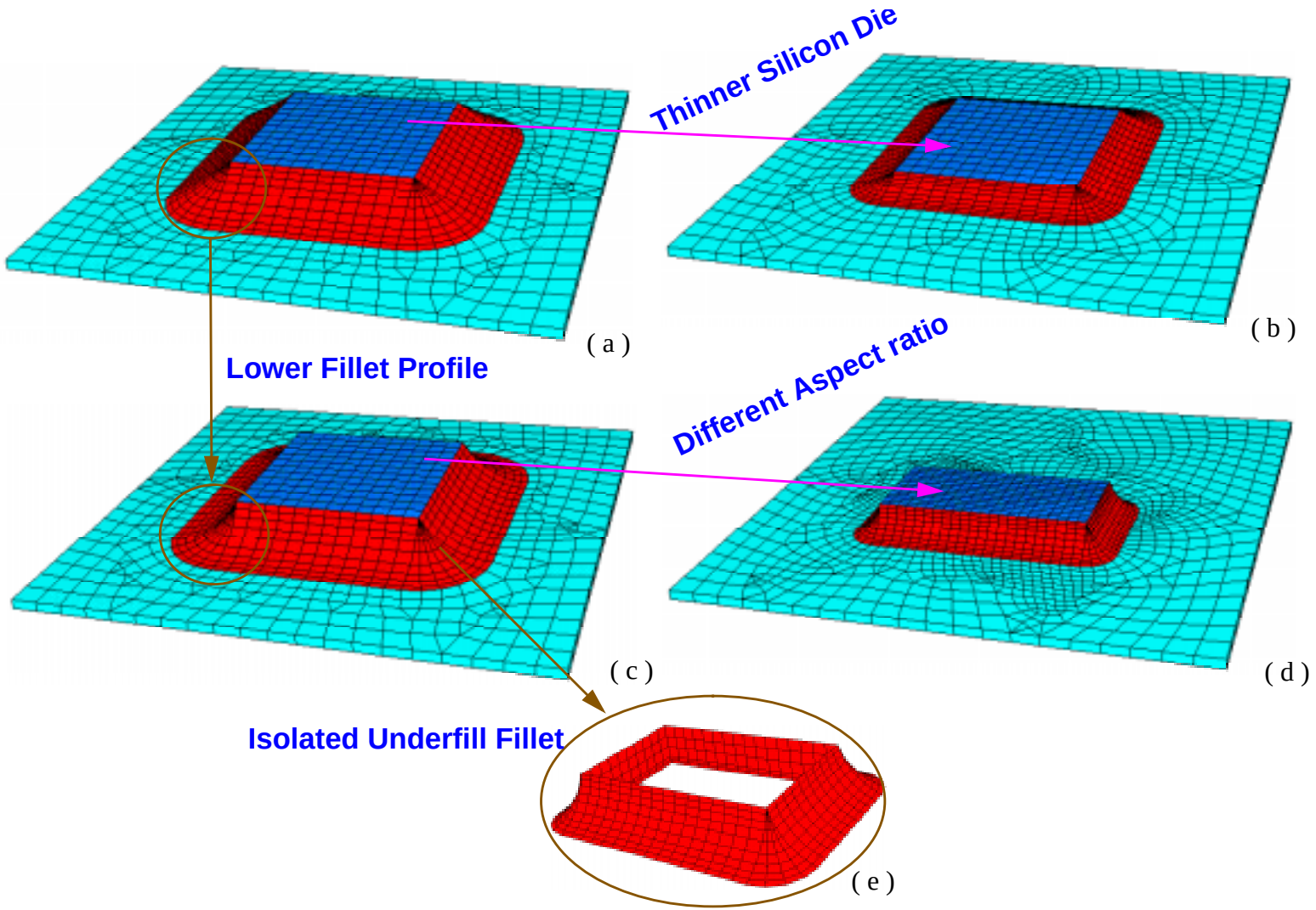


Figure 7.3 Parametric modeling of a DCA component.

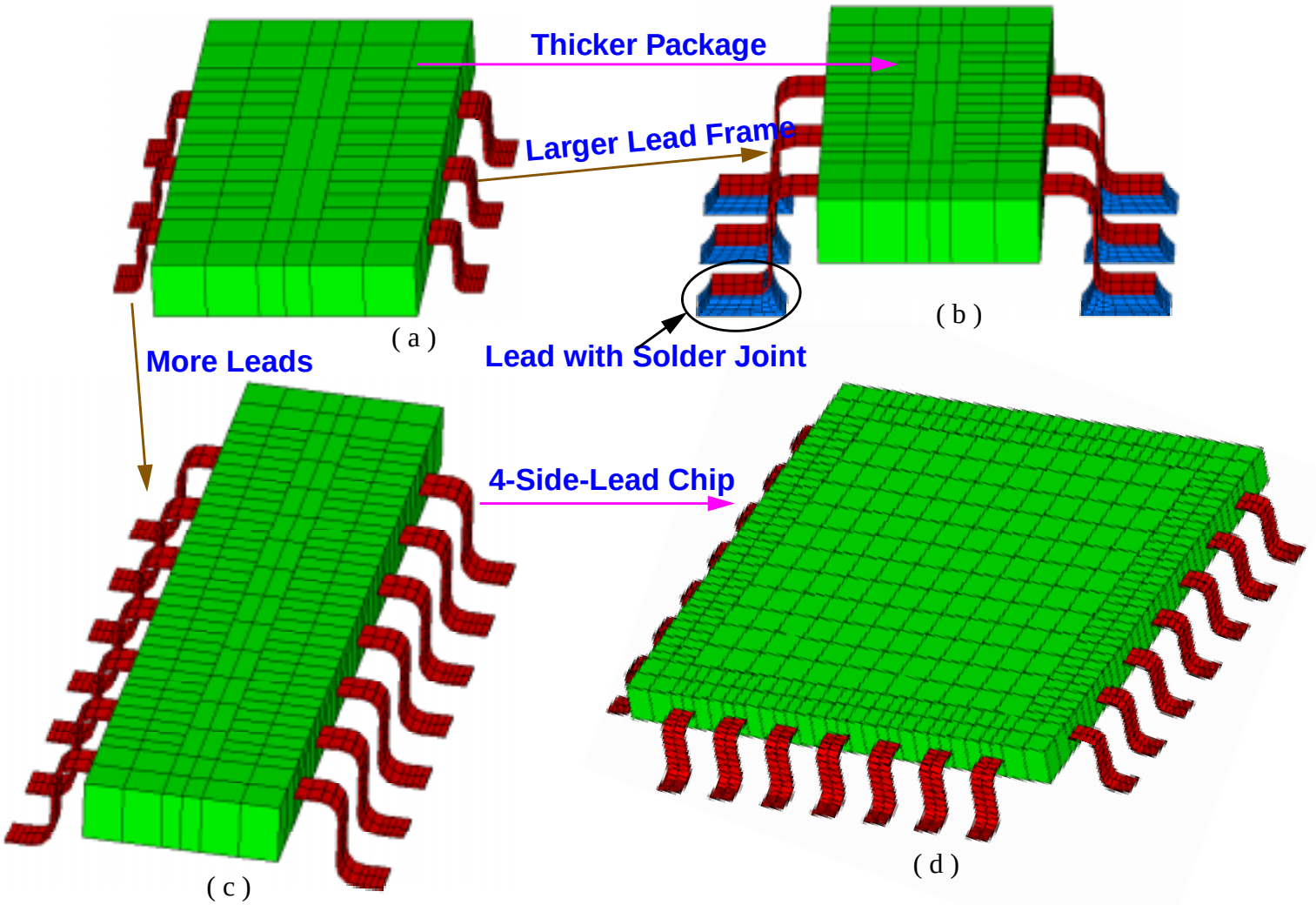


Figure 7.4 Parametric modeling of a TSOP component with gull lead

increased. As the size of package is dynamically calculated by number of lead frames, the package will match this changes of lead frames. In case (d), the parameter of No_of_sidelead is assigned as 4, which instructs the program to create four side lead-frame, instead of two.

Similar to Figure 7.4, four TSOP with J lead are showed in Figure 7.5. It has to be noted that when performing the operation of attaching a solder joint to leadframe, the selection of solder joint module type is dependent on the link specified on CMAT graph, described on chapter 5.

7.3 Component and Material library

7.3.1Component Library.

Since the component model saved in a CAD system preserve the geometry and topology, the same model and its associated mesh information can be reused, as long as the physical properties remain the invariant. When the finite element analysis for the component is required, the user may request the information stored in the CAD system by inputting a Constructive Module (CM) tree for that component. Hence, the model of the component, once created with the help of a solid modeller, can be stored in a CAD system, and reused for another component that is geometrically and topologically equivalent to this master model.

In mechanical analysis, these electronic products may be treated as an assembly of typical components, which can be classified and saved into a mechanical component library. Each component can be defined as a finite element module. This module is different from a meshed FE model, as its geometry, mesh shape, and density are created by parameters and form rules. Each module may have different types of analysis capability, such as static-structural, static-heat transfer, transient heat transfer, or modal

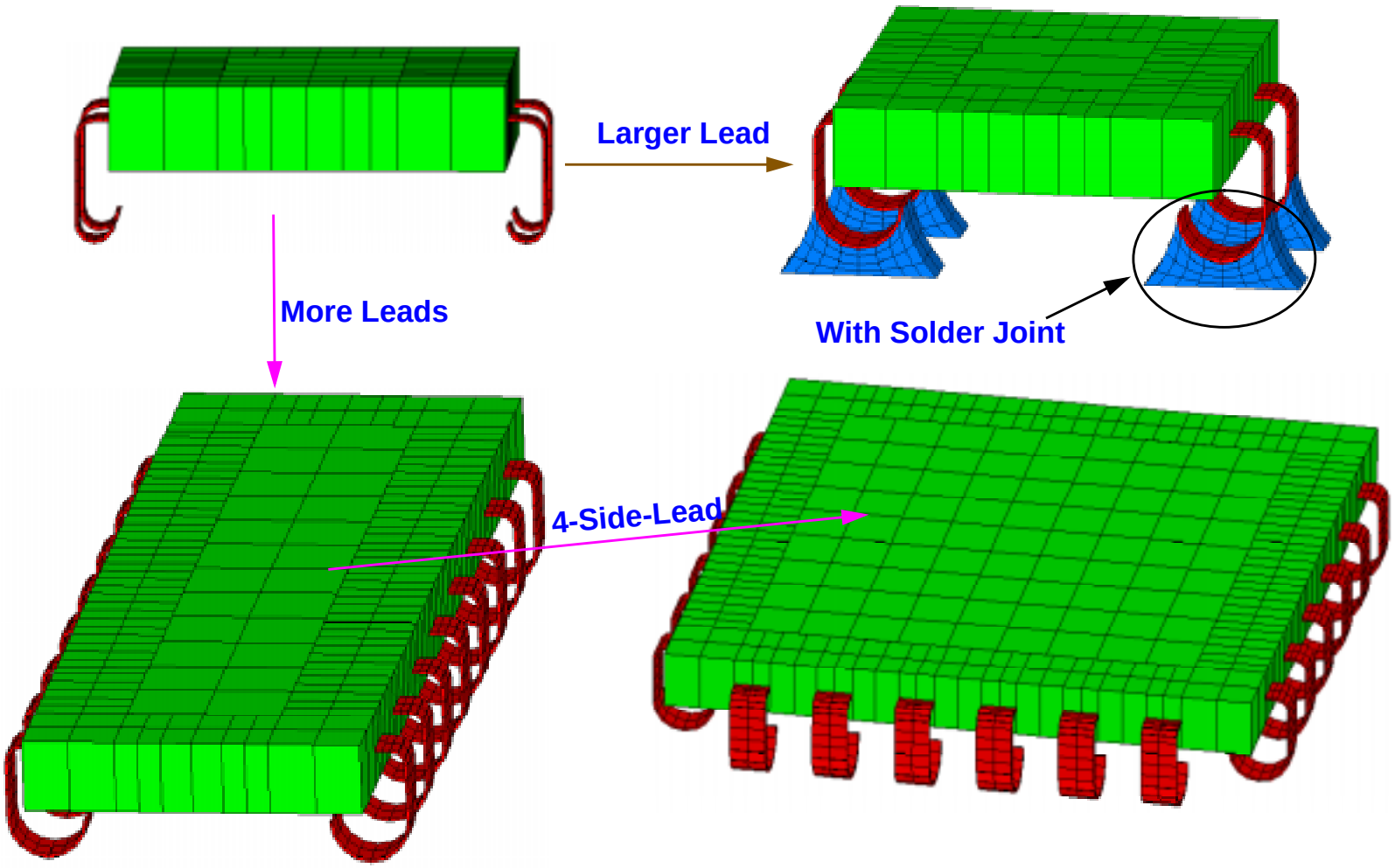


Figure 7.5 Parametric modeling for a TSOP component with J lead.

analysis. Each module may be further encapsulated into a higher level module. Using these standard parts (models) will reduce the number of components that must be generated from scratch. The original model-primitives in the component library, after initial construction, will never have to be remodeled. These model-primitives are generated and validated by expert, and lately, would be used by product designer to create a model for predictive analysis.

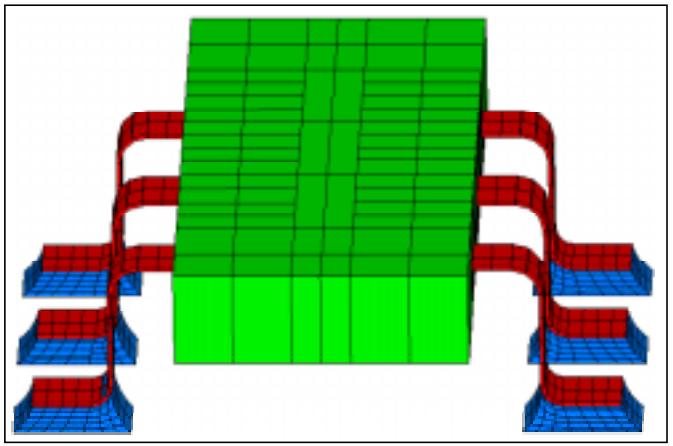
It is important to note that both component module and its pre-defined parameters are saved in the component library. The parameters include not only geometric parameters, but also parameters for materials, mesh control, analysis type, and assembly control. These parameters are categorized, and linked with different resources. For example, the geometric parameters are linked with user input by, the material parameters are linked with a database, etc. Figure 7.6 show a TSOP component and its different data groups.

7.3.2 Material library

Development of a material database can be a means to achieve 10x reduction in cycle time and provide a means to integrate with analysis tools. Depend on the needs and accesses of a material database, several database prototypes may be used to simplify the material look-up process. It can be saved in computer format as a hard copy of material handbook. The data are sorted and classified by material name and type, and mechanical and electrical property. Either relational database or object oriented data base theory may be applied.

For the purposed of modeling and analysis, in the thesis scope, the material database is developed as an external file, which includes material name and their numerical value. The file is linked with FEM program by material name. The data is read by matching the material name and ID number.

The material library includes properties for various package elements including



Geometry Data

- Component_List
- Component_Type
- No_of_Lead_side
- Package_Length
- Package_Width
- Package_Thickness
- Lead_Pitch
- Lead_Width
- Lead_No_x
- Lead_No_y
- Lead_Type
- Lead_Should
- Lead_Height
- Lead_Base
- Solder_Fillet
- Solder_Height

Material Data

E, G, γ, α, UTS, ρ, κ, c,.....
- Plastic_Compound
- Lead_Material
- Solder_Joints

Mesh Control Data

- Element Type, Size, Density, Shape.
- Node and Element Relations
- Constrain Equations

Assembly Control Data

- Component_Location
- Orientation
- Substrate_Size
- Neighboring_Component

Analysis Control Data

- Analysis_Type
- Element_Type
- Convergence_Criteria

ECAD System -2D Layout

ECAD System - Component Library

ECAD System - Not Available So Far

Component Vendor - Catalog

Deafaults & Expert System

Outside Link - SINDAS Datbase

Defined by User Request

Figure 7.6 A TSOP component and its parameter (data) groups.

die or chip; first-level interconnects; and device packaging materials. These properties provide a basis for selecting materials for different package elements, and also form inputs for the physics-of-failure models used in reliability assessment. When a mechanical component (or module) is picked for an analysis, its material properties will be also taken from the material properties database. A material sensitivity study may also be performed by changing to other material candidates. Based on result, other material in the database may show better performance. This alternative may be provided to the designer for optimization. The unitization of material database is demonstrated through the case studies, in chapter 9 and 10.

7.4 Global/local analysis

Global/local analysis provides the capability for different levels of analysis. Two different types of analysis are applied in global and local analysis: structural analysis and reliability prediction. Structural analysis evaluates the characteristics of package architecture in terms of stress/temperature distribution, and hot spots on PWBs or substrates for geometrically coarse representations of the system. Structural analysis is to provide first-order insight into the behavior of the system, to determine the parametric sensitivities and inflection points and to confirm that the final design can perform within the imposed specifications. The information obtained at this level will be the input for calculating the stress concentration and distribution, and for reliability prediction of particular interested part of a package. The reliability analysis calculates the time to failure for dominant failure mechanisms in a assembly. For different failure mechanisms, formula based tools are applied at this level of analysis.

For an electronic product, it includes very complex geometry and thousands of tiny parts. Producing detailed results for the entire product is neither possible nor necessary. During the first step of the global/local analysis procedure, the intent is to capture

a global behavior when a whole product model is present. The global results may be warpage, stress or strain distribution, or “hot spot” on the product. The results may be approximated, but could indicate trouble spots for more detailed analysis. By focusing on a spot of interest, other parts are removed from its boundary, and previous results are applied as a boundary load. More detailed analysis is then performed on this part. Based on this detailed analysis, a formula based calculation can be performed to predict reliability data. A global/local analysis example is showed in Chapter 10.

Chapter 8

Divided-and-Conquer Modeling Approach for Multi-layer PWB

In this chapter, a divide-and-conquer algorithm is developed to model a multi-layer PWB substrate with copper traces. Section 8.1 describes the importance and difficulties for creation a FE model of multi-layer board with copper traces. Section 8.2 introduces the divided-and-conquer algorithm. This algorithm will partition the board into small sections, such that each section can be individually modeled and assembled back to represent the original board. Each small section is still a multi-layered structure with an orthotropic copper-trace layout. The mechanical behavior of a small section is studied in Section 8.3. Section 8.4 introduces a window clipping algorithm to perform partition operation. Section 8.5 performs a FE analysis for a multi-layer board with an orthotropic copper trace layout.

8.1 PWB Description and Problem Definition

The most commonly used substrate for surface mount assembly is Printed Wiring Boards (PWBs). The PWB provides the physical platform for electrical components, and their electrical interconnection for circuit operation. The PWB is a complex, laminated, multi-layered assembly. It composed of alternating layers of copper and electrical

material. Due to the mismatch of their coefficient of thermal expansion, thermal expansion can cause PWB warpage during manufacturing process and during actural operations. This warpage can create long term reliability problems of micro electrical product. Furthermore, as PWBs are the platform of electrical components, the mechanical integrity of the board and the components mounted has to be treated as single unit. The mechanical behavior of a PWA is determined not only the components, but also the board and their connections. An isolated analysis model, without the concern of the entire board, is hard to capture the global effects, and sometimes, tends to give misleading results. Thus, it is essential that an accurate model be built to predict the mechanical behavior of PWBs.

8.1.1 General description of PWBs lay-up.

Most PWBs are composed of layers of fiber glass and copper. The number of layers, which can be vary from 2 layers to 40 layers, is dependent on the application. The copper plane provides the necessary circuitry for transport device signals. The connections of the copper traces in different layer are generally joined by vias. The copper trace layout in one plane is determined by electrical function design. The trace width may vary from 1mil to 10 mils and height from 2mils to 5 mils, based on the needs and cost of an application. Since electrical functions determine the copper trace layout, it is impractical to characterize the geometric representation of the copper traces.

8.1.2 Difficulty and complexity of FE modeling for PWB.

The complex, almost arbitrary, trace layout and highly distorted aspect ratio of trace to board propose a large mount of difficulties for mechanical engineers to describe the PWBs' structure in a simple manner. Consequently, a practical model, that can be solved at reasonable time and expenditure, can be hardly developed. The most hardest parts that can not be handled by traditional mechanical modeling approaches are as

follows:

1. Complexity of copper trace distribution and orientation. As mentioned in previous sections, the copper traces layout is determined by electrical design, and it is very difficult to find general rules for describing their geometry layout. In addition, the layout of copper trace vary significantly in different applications.

2. variation of material properties. Characterization of material properties for PWBs is hard to conducted. Due to the complexity of copper trace, the material properties vary in different location. In practice, the determination of mechanical behavior is only based on experimental testing of a small PWB section, which is cut from the board. The data obtained through the testing is the effective value of a composite structure. The smallest size of a specimen that can be conducted in testing, currently, is about 1/4x1/4 inch. Because of the copper distribution and orientation, the tested material properties can only represent the location, where the specimen is cut. Thus, the material properties obtained is very regional.

3. Distorted geometry aspect ratio. The board size is large, compare to its thickness. Usually, the size of a board size is measured in the unit of inch, while board thickness is in mils, and copper trace is in percents of mil. In addition, the board may compose more than ten alternative layers of copper and fr4. The aspect ratio of individual layer to the thickness of copper may greater than ten thousand. Creation of a FE model for board structure by conventional techniques is practically impossible.

In order to address these confronted problems, an approach, so called divided-and-conquer method, is presented in the following sections.

8.2 Divided-and-conquer method

The divide-and-conquer approach is a well known algorithm in computer science. It is used to solve a complex problem of large size. This algorithm breaks the

problem into several sub-problems, similar to the original problem but smaller in size, solves the sub-problems, and then combines their solutions to create a solution to the original problem. In another words, this algorithm says if we can solve a problem of small size, we can solve it in big size. This algorithm will be used to model a PWB (substrate) with copper trace.

The divide-and -conquer paradigm involves three steps at each level of the recursions:

Divide: The problem into a small a number of subproblems.

Conquer: the subproblems by solving them recusively. If the subproblem is simple enough, just solve the subproblem in a straight-forward manner.

Combine: the solutions to the subproblems into the solution for the original problem.

The algorithm, used for modeling PWB, closely follows the divide-and-conquer paradigm (Figure 8.1). Intuitively, it operates as follow:

Divide: Continuously break the PWB into small sections, until each section is small enough, so that each section can be modeled as a multi-laminated FR4 with orthotropic copper trace layout.

Conquer: Based on the copper traces geometry and distribution within the cut section, a effective FE model is developed to represent the behavior of this section. This type of structure can be analyzed and solved by using match-of-inertia method, which is presented in next section.

Combine: After FE models for all sections are created, these FE models are combined together to represent the original PWB.

8.3 mechanical analysis of PWB section

In this section, a model is generated to resemble the actural structure of a cut section. Base on this model, an equivalent finite element is developed to calculate the

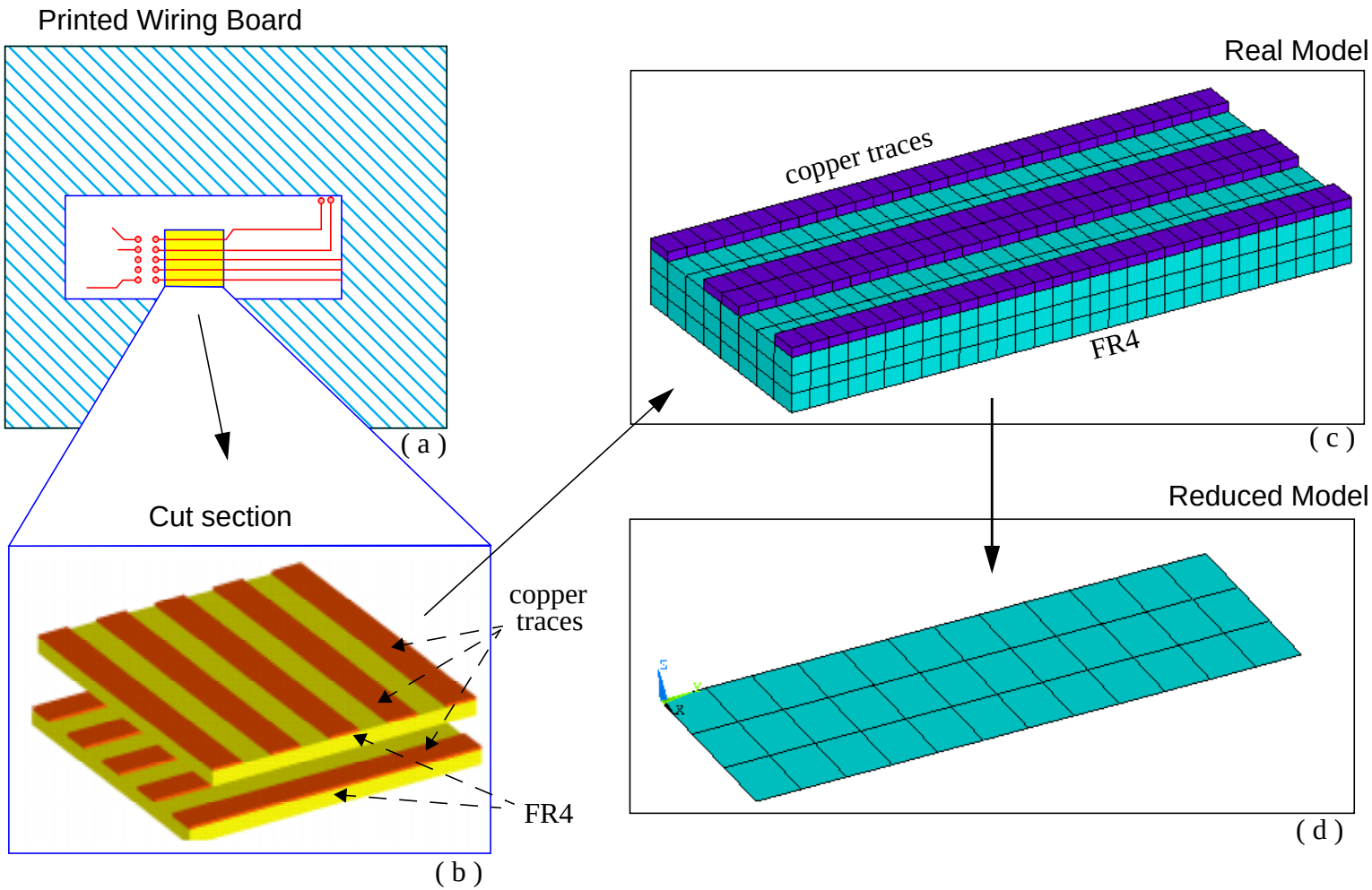


Figure 8.1 Divide-and-conquer algorithm for the modeling of a multilayer PWB.

deflection of the PWB. Later, an analytical model is derived. This analytic model is for more comprehensive study of cut section. Correlation between the warpage and temperature differential, change of overall temperature, and modules ratio can be qualitatively defined by this model.

8.3.1 FE structural modeling

Even for a small cut section, the geometric aspect ratio is still large. Simply meshing the structure by 3D elements will produce millions of 8-node element with 6-DOF. To overcome this difficulty, a match-of -inertia is used to simplify the modeling. The match-of-inertia is to replace the copper trace layer by a solid copper layer with modified material properties. This modification is necessary, due to the fact that the actual copper layer has othotropic property characteristics, as a result of material discontinuity in the direction perpendicular to the trace direction.

Since the major concerns are thermal and mechanical load, and the thickness of copper trace is much smaller than its length, the behavior of a trace is modeled as a cantilever beam under a pure bending moment. In the following model development, only a two layer board is considered, that is, it contains only a layer of copper and a layer of fiber glass.

The equation for the maximum deflection of a beam is

$$d = \frac{Ml^2}{2EI}$$

where M = moment, l=length of beam, E=Young's modulus, and I= are moment of inertia for a beam. To maintain the characteristics of the copper traces behavior under bending in the trace direction, the inertia of an uniform copper layer must be similar to that of the traces. This can be achieved by making the thickness of the uniform layer

one-half the thickness of copper trace. This is a very close approximation, when the thickness of the copper trace is much smaller than that of FR4. However, if it is not true, similar approach can still be used by finding the equivalent thickness. Referring to Figure 8.2, the approximation can also be derived from following equations:

$$I_{trace} = \int_{y_0}^{(y_0 + \Delta y)} w y^2 dy$$

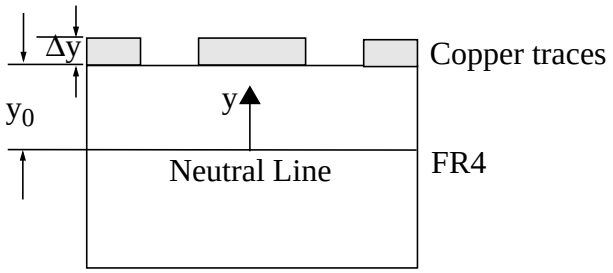


Figure 8.2 Cross section view of two layered board.

Where I_{trace} =area moment of inertia for trace, w=width of trace, y=distance from neutral axis to bottom of trace, Δy=thickness of trace.

$$I_{trace} = \frac{w}{3}[(y_0 + \Delta y)^3 - y_0^3]$$
$$= \frac{w y_0}{3}\left[3\frac{\Delta y}{y_0} + 3\left(\frac{\Delta y}{y_0}\right)^2 + \left(\frac{\Delta y}{y_0}\right)^3\right]$$

The are moment of inertia for a uniform copper layer is given as(1/2 of the trace):

$$I_{unif} = \int_{y_0}^{y_0 + \frac{\Delta y}{2}} 2 w y^2 dy$$
$$= \frac{w y_0}{3}\left[3\frac{\Delta y}{y_0} + \frac{3}{2}\left(\frac{\Delta y}{y_0}\right)^2 + \frac{1}{8}\left(\frac{\Delta y}{y_0}\right)^3\right]$$

The neutral axis is a little above the mid-line of the fiber glass (FR4). A FR4

layer generally has a thickness of 8 ~ 20 mils, while copper is just around 1 mil. Second and third terms in I_{trace} and I_{unif} are higher-order terms. When those terms are ignored, $I_{trace}=I_{unif}$. When several layers of copper and fiber glass are alternatively laminated together, the y_0 becomes much larger than Δy. Therefore, this approximation becomes more accurate in resembling the behavior of copper in trace direction. An additional modification is required for material in the transverse direction (perpendicular to the trace direction). Due to the discontinuity in this direction, The material property (Young' modulus) can be simply set as one-tenth of that in trace direction, and poisson ratio of 0.1. This modification is merely for avoiding numerical calculation errors.

After the determination of the equivalent thickness for the copper trace layer, the PWB section can be easily modeled by a layered element. Thus, a 3D structure is modeled as stacked 2D shell (c and d in Figure 8.1), but still maintains 3D behavior. However, the selection of a correct element type, which can represent the displacement and stress for a real structure, has an impact on the final calculation. For the case of a PWB under pure thermal and/or moment bending load, ANSYS STIF 91 element is selected. This element is a stretching-bending-shell element of 8-node with 6 DOF (Figure 8.3). In this element, a line that is straight and normal to the mid-surface before loading is assumed to remain straight, but not necessarily normal to the mid-surface after loading. Thus, transverse shear deformation is allowed.

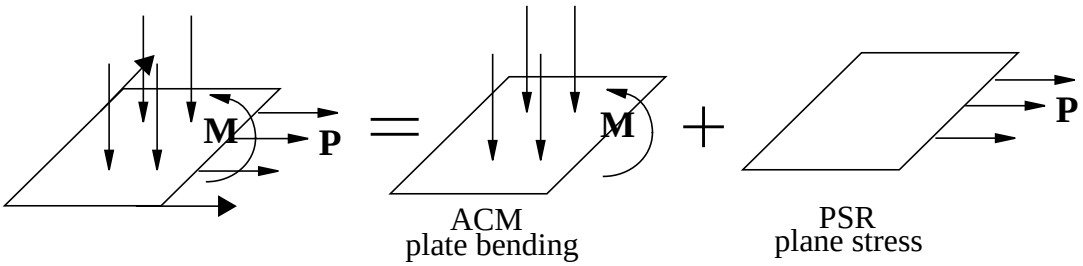


Figure 8.3 Selected stretching-bending shell element for PWB analysis.

8.3.2 Analytical modeling

The temperature loads create internal actions, or stress resultants, in the form of shear forces and bending moment, causing the plate to bend. Elaborate investigations of the strain show that for a thin plate or beam, warping of the cross section fur to shear strain does not substantially affect the longitudinal strain, even when the distribution of the load and shear force vary continuously along the length. This suggests that shear stress analysis can be neglected, and the warpage can be the only result of the bending moment. Also, because the ratio of plate size to its thickness is large than 100, it is reasonable to model the PWB under temperature load as a cantilever beam, loaded by a constant bending moment. For simplification, the deflection curvature of a two layered composite beam is derived. The materials of this beam are assumed to be linear elastic, and the deflection is assumed to be small. It is believed that the results can be used as an analog to analyzing the behavior of the PWB.

Suppose that the two layered beam is separated, so that they can be free to expand under temperature load. Let α_1, and E_1 denote the CTE and Young's modulus of beam one, and α_2 and E_2 for beam two. h_1 and h_2 are the thickness for each beam, and w is the width of the beam. The change of temperature in upper layer is ΔT_1, ΔT_2 for

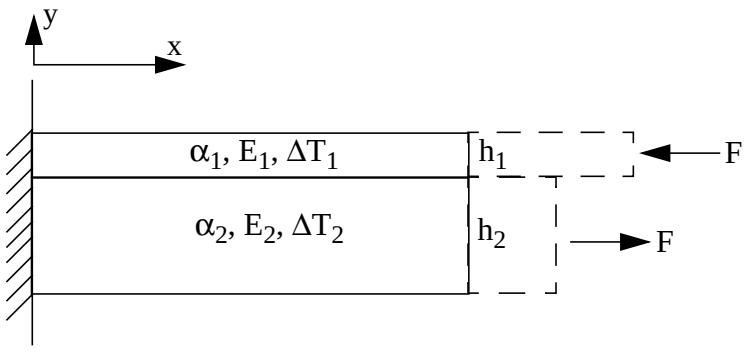


Figure 8.4 Two layered composite beam with thermal load.

lower one The beams are assumed to be perfectly insulated. Thus no heat conduction may occur. The straight longitude strain (x-direction) of beams are

$$\varepsilon_1 = \alpha_1 \Delta T_1 \qquad \varepsilon_2 = \alpha_2 \Delta T_2$$

Since the beams are so thin that the stress, which acts on the bottom of the upper beam due to the mismatch of the elongation of the two beams, can be equivalently represented by a horizontal force F. An equivalent same force applied to the lower beam, but opposite in direction. As a result of these two forces, the two beam yield in same strain elongation.

$$\varepsilon = \varepsilon_1 - \frac{F_1}{A_1 E_1} \qquad \varepsilon = \varepsilon_2 + \frac{F_2}{A_2 E_2}$$

Where A_1 and A2 are the cross section areas of the two beams.

The magnitude and force F and the bending moment M in the beam due to the force coupled can be expressed as:

$$F = (\alpha_1 \Delta T_1 - \alpha_2 \Delta T_2) \frac{A_1 A_2 E_1 E_2}{A_1 E_1 + A_2 E_2}$$

$$M = F\frac{h1 + h2}{2}$$

The next step in the analysis is to locate the neutral axis. The position of the neutral axis can be found by using the condition that the resultant axial force acting on the cross section is zero.

$$\int_1 \sigma_{x1} dA + \int_2 \sigma_{x2} dA = 0$$

Replace σ_{x1} and σ_{x2} by $\sigma_{x1}=E_1\kappa y$ and $\sigma x2=E_2\kappa y$, and denote the distantness from the axis to the interface of beam as D.

$$E_1\int_D^{(D+h_1)} ydy + E_2\int_{-(h_2-D)}^{D} ydy = 0$$

Solving this equation,

$$D = \frac{E_1 {h_1}^2 - E_2 {h_2}^2}{2(E_1 h_1 + E_2 h_2)}$$

Introduce the notation $n=E_2/E_1$, where is the modulus ratio.

The relationship between the bending moment M and stress in the beam can be derived as follows:

$$M = \int \sigma_x y dA = \int_1 \sigma_{x1} y dA + \int_2 \sigma_{x2} y dA = \kappa(E_1 I_1 + E_2 I_2)$$

Where I_1 and I_2 are the moment of inertia about the neutral axis of across section area one and two. The moment of inertia I_1 and I_2 about neutral axis can be found by using

parallel-axis theorem.

$$I_1 = \frac{1}{2}wh_1^3 + h_1w\left(\frac{1}{2}h_1 + D\right)^2$$

$$I_2 = \frac{1}{2}wh_2^3 + h_2w\left(\frac{1}{2}h_2 - D\right)^2$$

Finally, equation M=k(EI+EI) can be used to determine the curvature:

$$\kappa = \frac{1}{\rho} = \frac{M}{E_1I_1 + E_2I_2}$$

$$= (\alpha_1\Delta T_1 - \alpha_2\Delta T_2)\frac{n(h_1^2h_2 + h_2^2h_1)}{\frac{13}{6}(h_1^4 + nh_2^4) + nh_1h_2\left(\frac{2}{3}h_1^2 + \frac{2}{3}h_2^2 - 3h_1h_2\right)}$$

if $h_1 \approx h_2 = H$,

$$\kappa = (\alpha_1\Delta T_1 - \alpha_2\Delta T_2)\frac{12}{17\left(nH + \frac{H}{n}\right) - 10H}$$

if $h_1 \gg h_2$, and remove higher order terms,

$$\kappa = (\alpha_1\Delta T_1 - \alpha_2\Delta T_2)\frac{h_2}{h_1^2}n$$

The assumptions $h_1 \approx h_2 = H$ and $h_1 \gg h_2$ represent two cases in the PWB analysis. Since a board under thermal load will bend up or down, this effect of bending can be always be reproduced by a two-layer beam with appropriate material properties.

• $h_1 \approx h_2 = H$: The direction of bending can be analyzed by "breaking" a PWB into two layers, and studying the equivalently material properties of each layer. When a PWB contains more than a few layers, it can be treated as two equivalent layers. In this case, EQ 8.1 may be applied to predict the maximum deflection.

• $h_1 \gg h_2$:Let h_2 be the thickness of copper and h_1 be the thickness of fiber glass. In general, the thickness of fiber is much bigger than that of copper. When the question, "how the warpage varies with the amount of copper used, or the thickness of copper", has to be answered before a decision can be made, EQ 8.2 might be applied to give a qualitative answer.

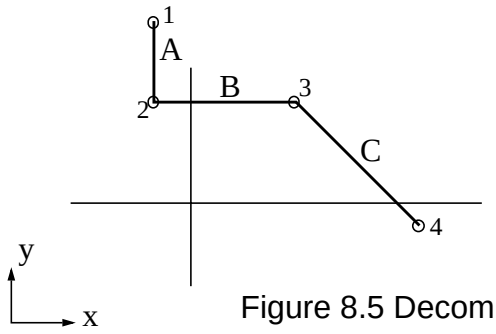
Though the analytical modeling approach is not directly applied in divided-and-conquer algorithm for the FE modeling of a PWB, it is helpful in understanding the correlation between PWB warpage and geometric parameters and material properties of a PWB, so as to develop a better model.

8.4 Clipping algorithm for section element

The preceding section discusses a FE modeling approach for a small section of a PWB. It is assumed that the copper distribution within the section element is known. However, given a complex PWB layout, finding the copper distribution and orientation for all section elements is not an easy task. The copper trace distribution has to be known, in order to develop a FE model. A clipping algorithm is used to determine the copper trace distribution and orientation of a cut section.

Given the boundary of a section element in a PWB, this algorithms is to clip out all the copper traces exterior the boundary, and to keep the trace segments inside boundary. It is assumed that the copper trace layout is described as a collection of trace lines. Each trace line can be decomposed into straight line segments. Each straight line

segment is defined by its two end points. For example, a copper trace, shown in Figure 8.5, can be decomposed into three segments, which are defined by three pairs of point set.



Line Segment A: (x_1, y_1) - (x_2, y_2)

Line Segment B: (x_2, y_2) - (x_3, y_3)

Line Segment C: (x_3, y_3) - (x_4, y_4)

Figure 8.5 Decomposition of a copper trace line.

Suppose that a section element is given as a rectangle, defined by its four corner points. Any copper trace within, or pass through the boundary of the rectangle, has to be kept, or clipped by the rectangle. Consequently, a trace line is divided into, at most, three connected trace lines. The total number of trace line in the collection is increased. But, each line segment, in the new collection, is either completely inside or outside of rectangle. The trace segments, inside rectangle, are used for developing an equivalent shell FE model for this rectangular section. The developed clipping algorithm is explained as follows.

A 4 bit array is allocated, for each end point of a line segment, to identify the relation of a line segment to a given rectangle. A line segment could be:1) completely inside, 2) completely outside, 3) partially inside, or, 4) pass through (Figure 8.6). Based on an identified relation, an appropriate calculation can be performed to find the intersection point of trace line and rectangular boundary.

The first bit of the array for a point represents the relation of if the point is below the top boundary of the rectangle. If yes, the bit has a value of 1, otherwise, it is 0. Similarly, the second represent bottom relation, the third for right, and the forth for left. If each bit array of a line segment is (1, 1, 1, 1), this line segment is completely inside of

rectangle. No clipping is needed, and just keep this line segment. If two bits array of a line segment have zero value on same array location, it implies that this line segment is completely outside of the rectangle. No clipping is needed, and just discard this one. For example, both (0, 1, 1, 1) and (0, 1, 0, 1) have zero value on first bit. It simply indicates that both end points of this line segment are above the top boundary of the rectangle. Thus, this line segment is discarded. If the line can not be treated as simply accept or discard. clipping calculation is needed to find the intersection point line segment and rectangle. For each bit in an array for a end point of a line, zero value indicates clipping is needed. Zero value in bit one means intersection is on top boundary line of the rectangle. Calculation of two linear equations of top line and the line segment will result in the intersection point. Similarly, zero value in bit two for bottom intersection calculation, bit three for left, and bit four for right.

The pseudocode of the algorithm LCES (Line Clipping of Element Section) is written in below, and regions of different bit value is showed in Figure 8.6. Let the corner points of rectangle are (x_l, y_b), (x_r, y_b), (x_r, y_t), and (x_l, y_t), where, subscript l represent left, r for right, b for bottom, and t for top. (x1, y1) and (x2, y2) are the coordinates of two points of a line segment, and Bit[1][4] and Bit[2][4] represent the bit arrays of two points, correspondingly. The input collection of lines is assumed in the format of link list.

In LCES, Line 1 locates each line in the list; Line 2 executes SET_BITVALUE, which set the value of Bit array according the point location relative to the rectangle; Line 3 clips the line, if necessary, and add the clipped line to the line_list, which is the collection of line segments inside rectangle; Line 4 return the clipping result for all lines.

In CLIPPING, the variable sum1 and sum2 are used to check if all bit are equal to one. If sum1 and sum2 are both equal to 4, it implies that this line is completely inside rectangle, and thus, return this line without doing anything(Line 1-7). If any bit,

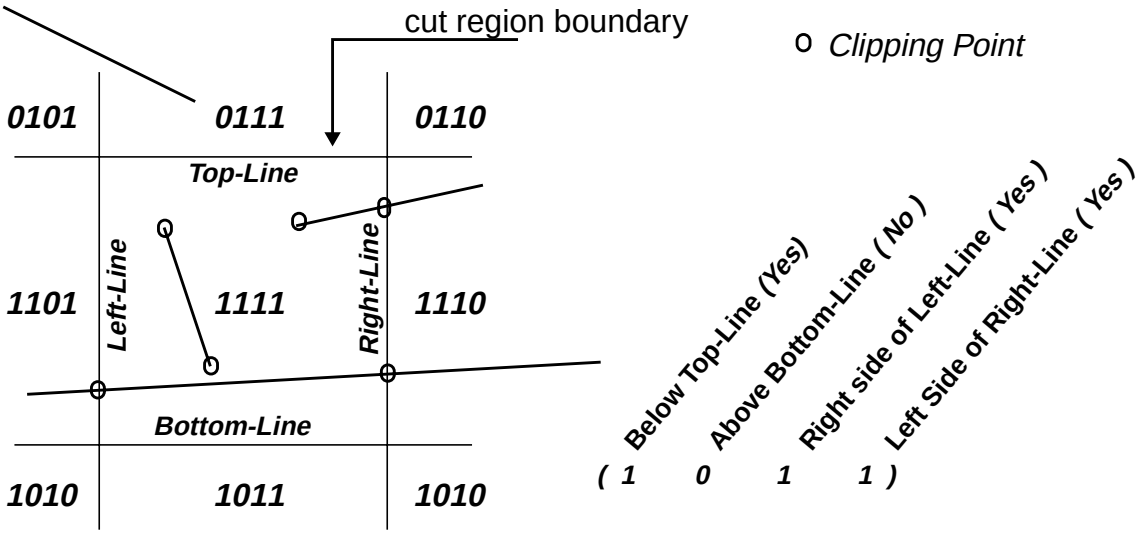


Figure 8.6 A bit arrary representation for defining boundary relation.

on same array location, has same value of zero, return Null, which means it does not count(Line8-10). Line 11 goes two ending point one at a time. Line 12 - 14 clips the line from rectangle's top boundary. Point_inter is denoted as intersection point from the solution of two linear equation. The calculation is performed by INTER function, which is not included here. The two equation (for top line) can be expressed as

$$\begin{cases} y = yt \\ \dfrac{y-y1}{y2-y1} = \dfrac{x-x1}{x2-x1} \end{cases}$$

or, can be used in isoparametric forms. Line 14 replaces the point, which is out side of rectangle, by the intersection point. Similarly, Line 15 -22 check and clip lines by left right, and bottom boundary line. NEW_LINE creates a new modified line and reset the bit value for the points of the new line.

Line_List **LCES**(Line_List *Input_List*) ❁ (Line Clipping of Element Section)

1. ***for*** each *line* ***in*** *Input_List*

2. ***do*** **SET_BIT_VALUE**(*line*)

3. *Line_Keep_List* ← **CLIPPING**(*Line*)

4. Return *Line_Keep_List*

SET_BIT_VALUE(Line)

1. ***for*** *i* ← 1 to 2

2. ***do*** *Bit*[*i*][1 to 4] ← 0 ❁ Initialize bit value

3. ***if*** yi > yt ❁ above top boundary

4. ***then*** Bit[i][1] ← 0

5. else if yi < yb

6. then Bit[i][2] ← 0

7. if xi < xl

8. then Bit[i][3] ← 0

9. else if xi > xr

10. then Bit[i][4] ← 0

11. Return

CLIPPING(Line)

1. sum1 ← 0

2. sum2 ← 0

3. for i ← 1 to 4

4. do sum1 ← sum1 + Bit[1][i]

5. sum2 ← sum2 + BIt[2][i]

6. if (sum1 = 4) and (sum2 = 4)

7. then Return Line

8. for i ← 1 to 4

9. do if (Bit[1][i] = 0) and (Bit[2][i] = 0)

10. then Return Null ❁ return nothing, so Line_List remain the same.

11. for i ← 1 to 2

12. do if (Bit[i][1] = 0) ❁ zero value of bit one indicates this point is above the line

13. then Point_inter ← INTER(Top_Line, Line)

14. NEW_LINE(Point_inter, Point_i)

15. if (Bit[i][2] = 0)

16. then Point_inter ← INTER(Bottom_Line, Line)

17. NEW_LINE(Point_inter, Point_i)

18. if (Bit[i][3] = 0)

19. then Point_inter ← INTER(Left_Line, Line)

20. NEW_LINE(Point_inter, Point_i)

21. if (Bit[i][3] = 0)

22. then Point_inter ← INTER(Right_Line, Line)

23. NEW_LINE(Point_inter, Point_i)

24. Return Line

NEW_LINE(Point_inter, Point_i)

1. Line ← Point_inter |+| Point_i ❁ update current working line.

2. SET_BIT_VALUE(Line) ❁ Reset the bit value for ending points of new line.

3. Return

The algorithms, developed above, are based on the assumption that each copper traces are composite of small straight line segments, and each line segment is given by its two ending points.

8.5 FE modeling for section element

A small PWB sample, provided by IBM, is used to test the FE model for a

clipped element section developed in previous sections. The geometry and configuration used of the testing board is shown in Figure 8.7, The copper layer is chosen from a stand size, which is specified in (oz/ft2), and is typically available in 0.5, 1.0, 2.0, 3.0 oz/ft2. The copper traces in each layer has only one direction. There are large amount of traces in each copper layer. Both trace width and trace separation are 5 mils. The fiber glass is glass-reinforced epoxy. It is an orthotropic material, which is specified by fill and warp direction.

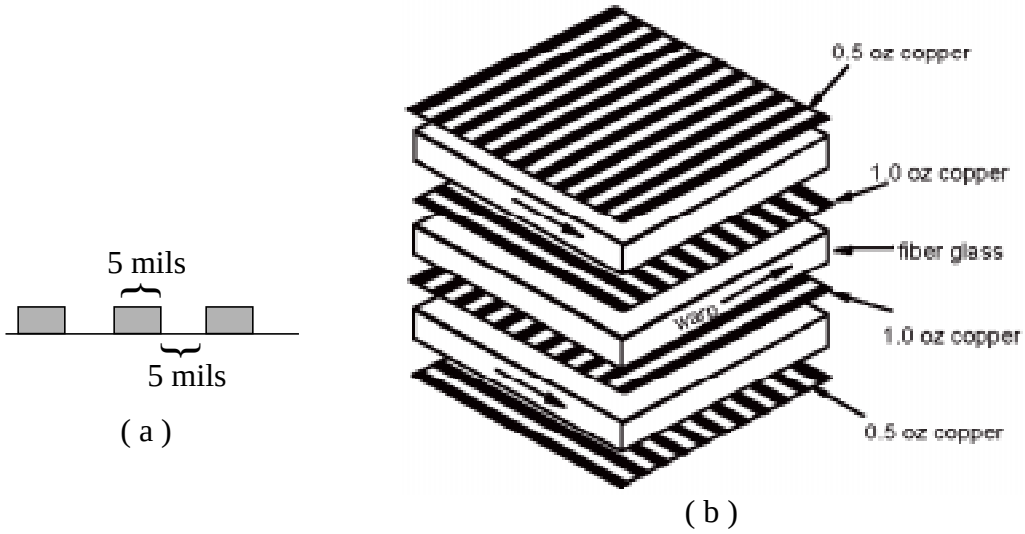


Figure 8.7(a) Cross section view of copper layer.
(b) Geometry and configuration of PWB sample.

Similar to the "free body diagram" used in statistic dynamics and mechanics of material, a small piece of structure is taken out to do the analysis. The behavior characteristics are extended to the overall structure. 930 elements are used to mesh the structure. The boundary condition is that every node on the leftmost end is clamped. The thermal load is attributed to a change of temperature from 20^{o}C reference temperature to 80^{o}C. This boundary condition and thermal load are applied to the developed model. 36 element are used for the reduced model, developed in section 8.3. In each

calculation, convergence has been tested to make sure the number of elements are enough to produce meaningful results. The computed deflections from these two groups are plotted against the distance of sample points to clamped boundary (Figure 8.8). The comparison of these results shows that the developed model can use a considerably small amount of elements to reproduce the results which use a tremendous number of elements to mesh the detail of the structure. In addition, curve fitting suggests that data curves in Figure 8.8 are pretty close to a quadratic curve. This demonstrate that the deflection of the PWB with only temperature load can be modeled as a beam with a bending moment

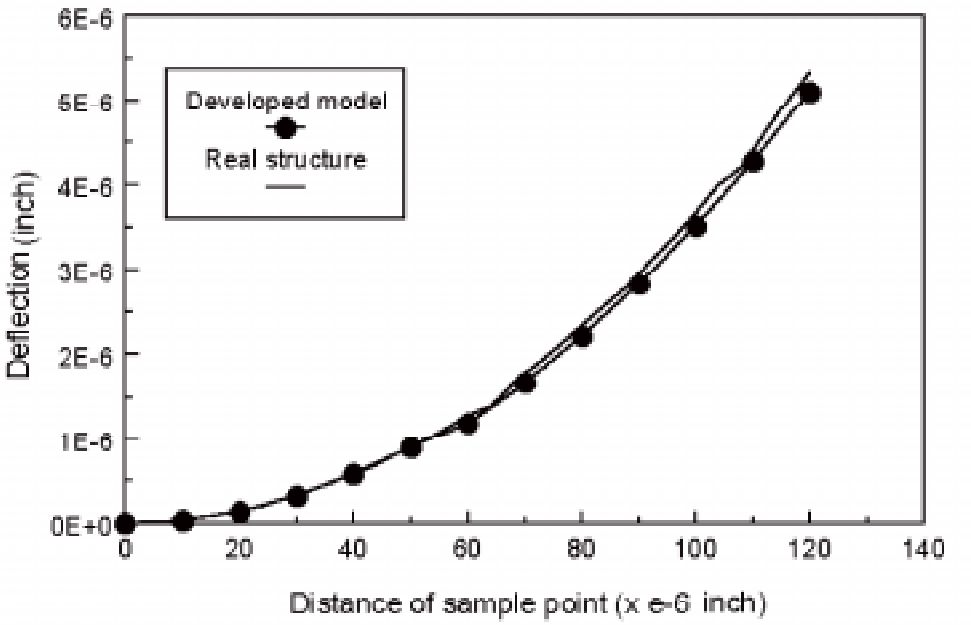


Figure 8.8 Comparison of a detailed FE model to a reduced model.

represented by EQ8.1

Based on the developed model with shell elements, a FE model for the entire PWB sample is created. The core material properties of this PWB are shown in Figure 8.9. These material results and measurement are contributed by fellow project member Jeff Garntt.

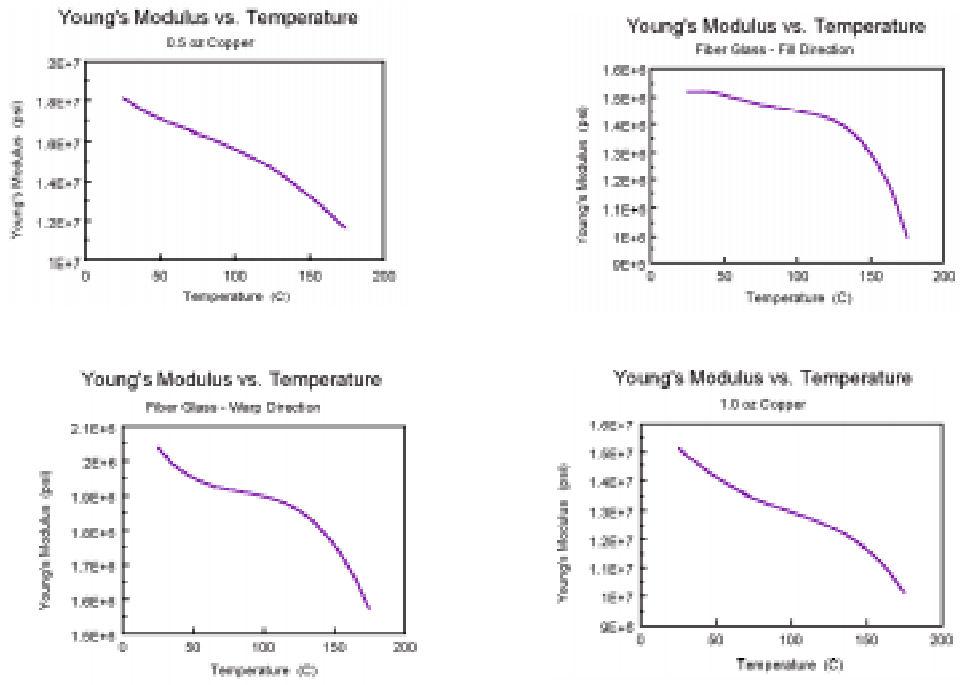


Figure 8.9 Material properties used for testing developed FE model.

The developed model is used to predict the maximum deflection of a board in a heating oven. Figure8.10 shows a board deformed shape when the board is put into a heating oven. The oven temperature is 125^{o}C, and room temperature is 20^{o}C. Due to the heater is under the board, the temperature on the bottom of the board is 10^{c}C higher than on top. The numerical results obtained by this approach have been compared with experimental results. It is found the warped shape is consistent with experimental observation, but the maximum deflection have 5 - 30% difference. It is believed this is due to ignorance of other factors in developing the model, such as initial warpage, moisture effect, temperature differential cross the board.

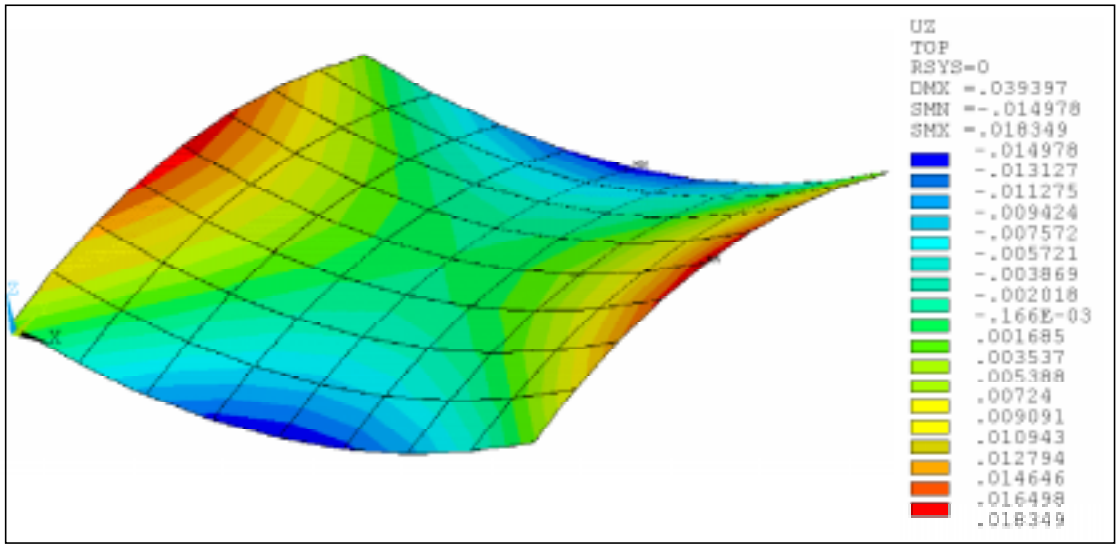


Figure 8.10 Warpage plot: Deformed PWB in a heating oven.

Part III

MP/FEM for thermomechanical modeling and Analysis of Electronic Packaging

Based on the developed methodology, two case studies are conducted. The first case study, parametric FE modeling for flip-chip on board, presents a systematic analyses based on the predefined parameters. The parameters include geometry size, initial conditions, loading conditions, materials, and optimization criteria. The second case study, MP/FEM for a board-level thermomechanical analysis, demonstrates the capability and flexibility of the methodology in model generation and model solution. A detailed FE model is assembled for a populated board. Different types of analyses, including global/local analysis, are performed.

Chapter 9

Case Study One: Parametric Finite Element Analysis of Flip Chip On Board Reliability

With increasing demands on low cost, miniaturization, weight reduction of future portable electronic products, flip chip on board (FCOB) technology has become a very attractive solution that can reduce die real estate area up to 90% compared with conventionally packaged die. In addition, FCOB technology is especially advantageous in high speed applications due to low interconnect inductance. Solder joints, the most widely used FCOB interconnects, have a relatively low structural compliance. Studies have shown that low structural compliance normally reduces solder joint fatigue life under thermal cyclic loadings. The reliability of FCOB assemblies can be enhanced by applying an epoxy-based underfill layer between the chip and the substrate, enveloping the solder joints. However, over ranges of design and process parameters, different failure modes are observed with significant dependence on material properties. Depending on the dominant failure mode, assembly structure optimization varies. However, over ranges of design and process parameters, different failure modes are observed with significant dependence on material properties.

A comprehensive parametric finite element analysis, by using MP/FEM developed in this thesis, for FCOB structures has been conducted to investigate the reliability

impact due to a number of selected design/process parameters. These parameters include PWB thickness, underfill thickness, die thickness, die size, initial PWB warpage, and underfill fillet profile. The study results have been validated through available experimental data published elsewhere.

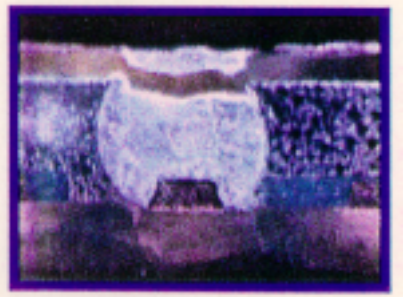
9.1 Introduction

Flip chip on board (FCOB) technology, also called direct chip attach (DCA), or flip chip attach (FCA), has recently received increasing attention as a way to improve package density and electrical performance. Compared to the similar but more mature C4 (Controlled Collapse Chip Connection) technology that requires reflow temperature up to 320 ^{o}C for lead-rich tin/lead (3/97) solder bumps, the FCOB process involves a lower temperature reflow temperature by using eutectic solder (63/37 tin/lead alloy) to join the chip solder bumps to the substrate. For this reason, the FCOB process can be used for the traditional low cost organic, epoxy-based printed wiring board (PWB) assembly process. Although the FCOB technology provides definite advantages over the C4 and traditional SMT packaged component assemblies, reliability concerns have been raised due to a higher coefficient of thermal expansion (CTE) mismatch between the silicon die (around 3-4 ppm/C) and the organic substrate (16-26 ppm/C).

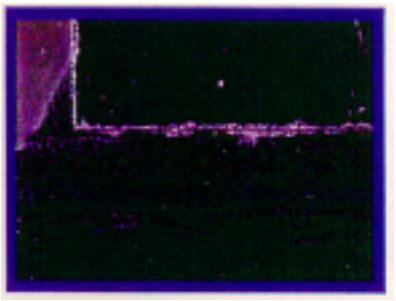
A significant number of reliability studies for the FCOB assemblies has been performed over the past few years. These studies, however, are based on design of experiment (DOE) approach. Table 9.1 tabulates the most commonly observed failure mechanisms. Based upon author's experience, during the early process development stage, items 1, 2, 3, and 5 are the most likely dominating failure mechanisms/modes. Six common failure mechanisms are shown in figure 9.1. As the FCOB process becomes more stable and mature, items 2 and 4 are more prominent.

Although the DOE-based approach has been proved to be a useful vehicle for

Deformed solder joint



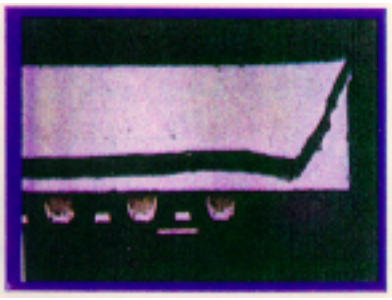
Delamination



Incorrect encapsulant fillet

Polyimide peeling

Encapsulant voiding



Cracked Silicon

Figure 9.1 FCOB reliability: failure mechanisms

process characterization and optimization, it involves construction of many prototypes. This is a very time consuming and expensive process. In addition, testing alone sometimes results in “trial-and-error” and “ad-hoc” experimental procedures. This, in combination with inherent testing noise, in many cases, may cause one to reach erroneous conclusions when extrapolating experimental data for new designs/processes that are different from the specimens tested. Most importantly, testing without analytical

simulation would not provide sufficient understanding and insight of the physical behaviors of the structures. Experimental data inevitably reflects the combined effects of a wide variety of factors, while it is the knowledge of the role of each particular design/ process parameter that is needed for reliability prediction. For these reasons, a comprehensive parametric finite element analysis has been proposed and implemented. Compare to conventional FEM, which has to re-modify FEM code each time when design input changes, MP/FEM is able to set design parameters into FEM code. Thus, the computer solver can automatically go through all these design parameters, without human interface. Design cycle time can be reduced, and more complete design and analysis can be performed. The subsequent sections describe the modeling approach and results.

Table 9.1. FCOB failure mechanisms and root causes.

Item	Failure Mechanisms (Modes)	Root Cause
1	Die Cracking (cracking initiated at the backside and the side walls of the die and propagated through die active area.	1. Edge defects due to inappropriate edge sawing. 2. Pitting on backside of die caused by mishandling. 3. Over-stress due to improper board design.
2	Delamination between die passivation and underfill (electrical open due to separation at solder joints).	1. Contamination and/or reactive chemical agents on the passivation. 2. Fatigue caused by cyclic loadings.
3	Delamination underfill and PWB solder mask (electrical open due to separation at solder joint).	1. Contamination and/or reactive chemical agents on solder mask.
4	Solder joint fatigue or creep (open due to solder fracture)	1. Fatigue caused by cyclic loadings. 2. Accumulation of creep cavitation damages.

Item	Failure Mechanisms (Modes)	Root Cause
5	Premature solder fracture (open due to fracture)	1. Stress concentration caused by voids, insufficient solder volume, misalignment, etc. 2. Debonding caused by interfacial contamination.

9.2 Parametric Finite Element Analysis

The objective of this parametric FEA study is to: (1) demonstrate the capability and flexibility of MP/FEM with emphasis on parametric modeling; (2) investigate the reliability impact due to various geometric design parameters, material properties, process conditions, and modeling techniques; and (3) construct a sufficient knowledge base in an attempt to develop comprehensive FCOB design guidelines for reliability enhancements. From this study, qualitative comparisons between different parameters will be performed and critical parameters will be identified. To obtain optimal reliability, design optimization has also been carried out. The parametric modeling, based on ANSYS finite element code, was used for this analysis.

9.2.1 Modeling Assumptions

1. Most efforts involved in this parametric study have been based on 2D linear elastic plane-strain analysis. To validate this assumption, both 3D linear and 2D nonlinear models were analyzed. In addition, experiments conducted independently by Motorola using laser moire interferometry have also confirmed that this assumption is valid over the temperature range studied.

2. To ensure that both the analyses and material properties stay in the linear region, an isothermal temperature loading swing from 100 to 25 ^{o}C was used.

3. All material properties including coefficients of thermal expansion (CTE), Young's Moduli (E), and Poisson's ratio (n) are temperature independent, homogeneous, and isotropic except for the PWB, which is treated as an orthotropic material (different in-plane and out-of-plane properties)

4. Perfect bonding is assumed at all interfaces between heterogeneous materials.

5. The maximum effective elastic strain (EEP) or Von Mises strain was calculated and used as the indicator for determining the reliability of the structures.

6. No initial residual stress is considered in the model and the structure is at a zero stress stage. As indicated earlier, the purpose of this study is not to determine the absolute true stress in the FCOB structure but rather to conduct a qualitative-based comparative analysis for various design concepts selected.

9.2.2 Model and material properties.

Finite Element Models: A baseline finite element model has been established based on a typical FCOB reliability test vehicle used at Motorola. The geometry of the FCOB structure is shown in Figure 9.2. The size of the die is 340 X 340 mil. The PWB is made of FR-4 laminated layers. To minimize the CTE mismatch between the PWB and the silicon die, the underfill materials is composite material that consists of thermoset polymer mixed with silica fillers. A net temperature swing of 75 ^{o}C (from 25 to 100 ^{o}C) was used for all analyses unless otherwise denoted.

Material Properties: The mechanical materiel properties of the PWB, underfill have been measured using a Rheometrics Dynamic Spectrometer at different temperatures. The solder joint and silicon material properties have been extracted from public material databases(SINDAS). Because the applied temperature of 100 ^{o}C is below the

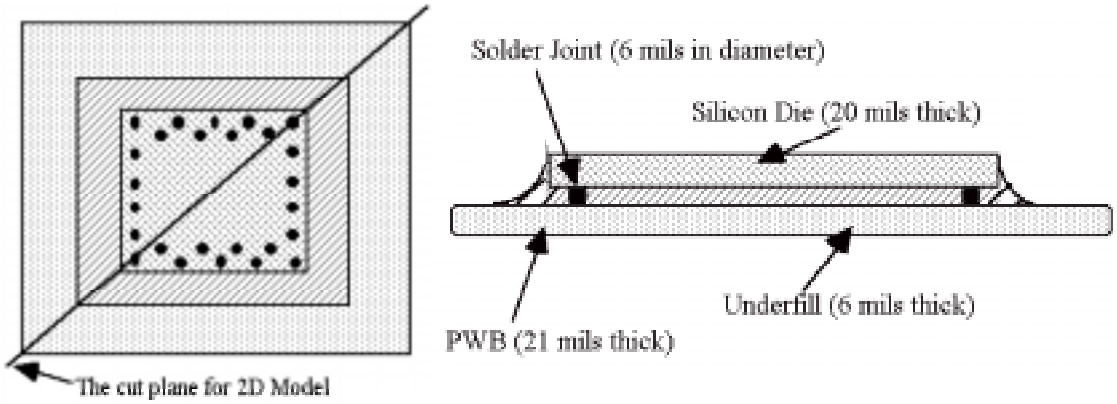


Figure 9.2: Schematic view of a typical FCOB structure

glass transition temperatures (T_g) of the PWB and the underfill (approximately 130 ^{O}C and 150 ^{O}C respectively), the material properties at room temperature were used with good justification. These material properties (below Tg) are tabulated in Table 9.2.

Table 9.2 Below Tg Material properties used for FEA

Material Properties	Silicon Die	Underfill	Solder	PWB
Young's Modulus (psi)	22.5E6	1.45E6	1.89E6	2.0E6 (in-Plane) 0.6E6 (out-of-plane)
CTE (in/in/C)	2.7E-6	26E-6	22.5E-6	22.5E-6 (in-plane) 60E-6 (out-of-plane)
Poisson's Ratio	0.3	0.33	0.35	0.35
Thermal Conductivity (W/m-^{O}C	150	2.9	48.6	27.2 (in-plane) 2.2 (out-of-plane)

9.3 Parametric FEA Study Results

The key parameters investigated in this study include temperature shock effects,

underfill thickness, die thickness, PWB thickness, solder joint location, die size, underfill fillet profile, initial PWB warpage, material properties, and 2D versus 3D models. Since the parameters used in models may be easily identified in different cases, they are not explicitly explained. The detailed results are described as follows.

9.3.1 Temperature Cycling Effects

The FCOB test vehicle normally undergoes a liquid-to-liquid temperature shock cycling testing. During the test, the structure incurs a large temperature swing (from 125 ^{o}C to -55 ^{o}C to 125 ^{o}C) in a very short period of time. It is of interest to understand the induced EEP resulting from such a temperature gradient during the cool-down and the heat-up stages respectively. A coupled transient heat transfer/structural analysis has been carried out to study the maximum EEP in the underfill and the corresponding temperature at the location where the maximum EEP occurs are calculated. As shown in Figure 9.3, the results show that there is a significant EEP variation (0.0052 to 0.0006) during the cool down cycle while the EEP remains stable at 0.0043 throughout the heat-up stage. Therefore, the cool down stage is more responsible for material fatigue than the heat up stage.

9.3.2 Underfill Thickness

As shown in Figure 9.4, a reduction in underfill thickness can increase the maximum EEP considerably in the underfill (42%), especially for the thinner underfill layers, but decrease the EEP only slightly in the die (6%).

9.3.3 Die Thickness

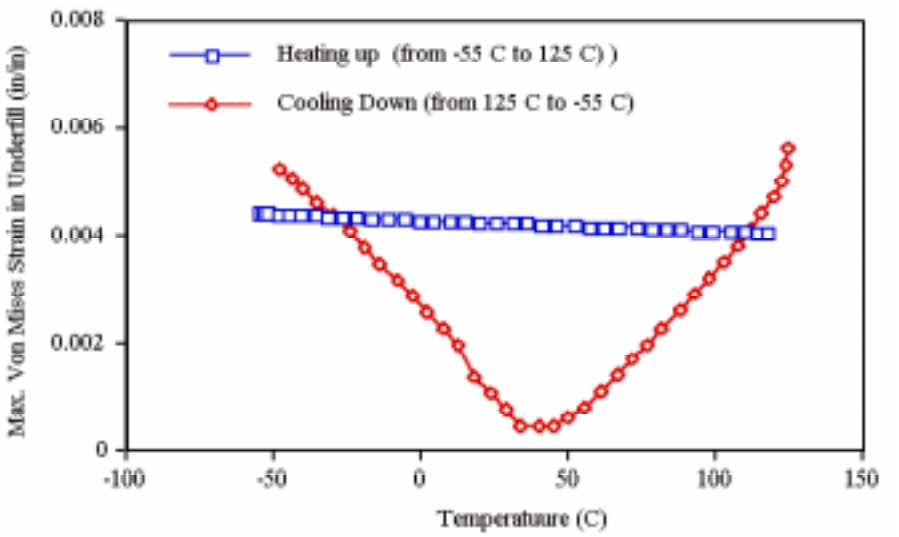


Figure 9.3 Maximum EEP in underfill (baseline configuration) during both cool-down and heat-up stage

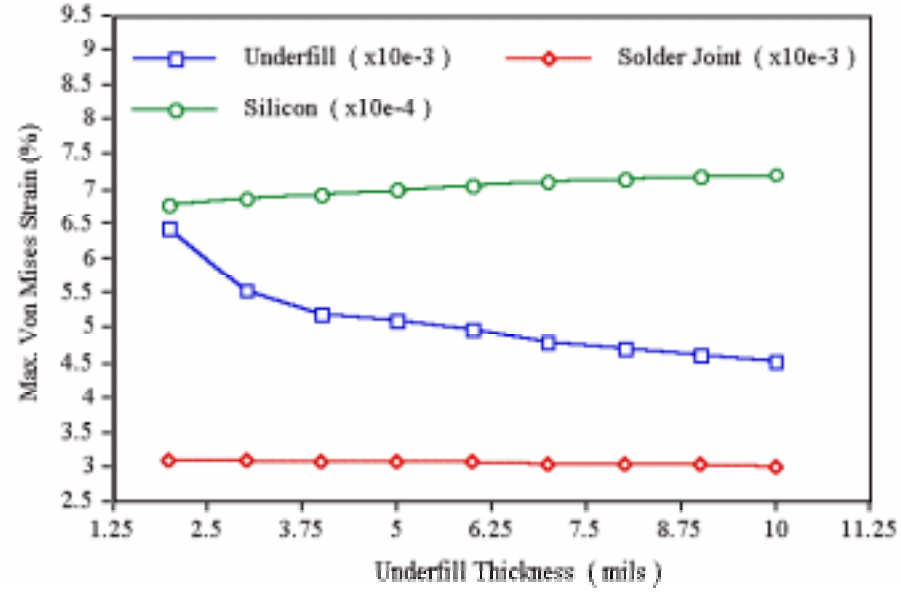


Figure 9.4 Parametric study results for underfill thickness.

As shown in Figure 9.5, the maximum EEPs in the die, underfill, and the PWB increases as the die thickness becomes larger. However, it should be noted that there

exists a local maximum EEP in the die even when the die thickness remains relatively small (approximately 15 mil).

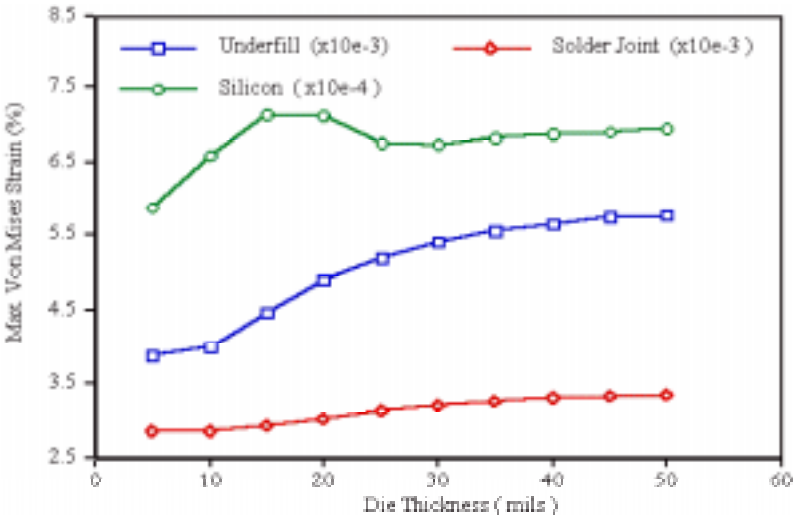


Figure 9.5 Parametric study results for die thickness

9.3.4 PWB Thickness

The parametric study result for the board thickness (5-50 mils) is shown in Figure 9.6. The maximum EEP in the die peaks when the board thickness is around 25 mil. The ratio of the largest and the smallest EEPs in the board thickness range studies is 33%. The maximum EEP of the underfill increases somewhat (12%) as the board thickness increases. The maximum EEP in the solder joint is insensitive to the board thickness variation (1% difference).

9.3.5 Solder Joint Location

The maximum EEP has been calculated for various distances (10, 15, and 20

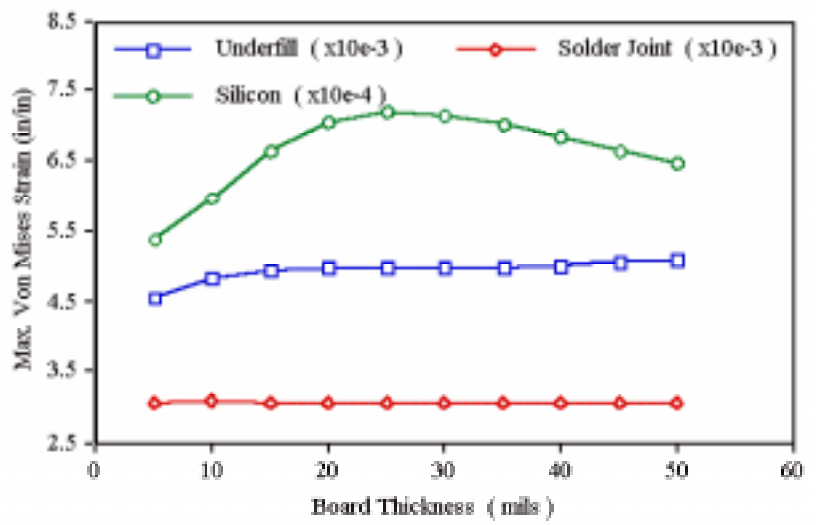


Figure 9.6 Parametric study results for board thickness.

mils) between the center of the solder joint and the die edges. It was found that the EEPs in the underfill and the die are insensitive to this distance. There is a very small EEP decrease (2%) in the solder joint as the distance become larger.

9.3.6 Die Size

The maximum strain in the underfill is often located at the interface near the lower corner of the die (Figure 9.7). In general, without underfill, the EEP in the solder joint for the larger die is much larger than that of the smaller die due to the larger DNP. Because of the laminated structure, the maximum EEPs in the underfill, the die and the board remain the same regardless of the die size and the DNP. It is also evident that the use of underfill can effectively reduce the solder joint strain by a factor of 2 to 2.5X. Based on the Basquin equation [1] below, it is predicted that the number of cycles to failure can be reduced to 4-10 X. This agrees with the results documented elsewhere [CLEM94].

$$N_f \gamma_e^{\beta} = \theta$$

Note that N_f is cycles to failure, β and θ are material constants. β is in a range of 2 to 2.7 for 60/40 tin/lead solder depending on the applied temperature [VAYN91]. γ_e is the calculated elastic strain.

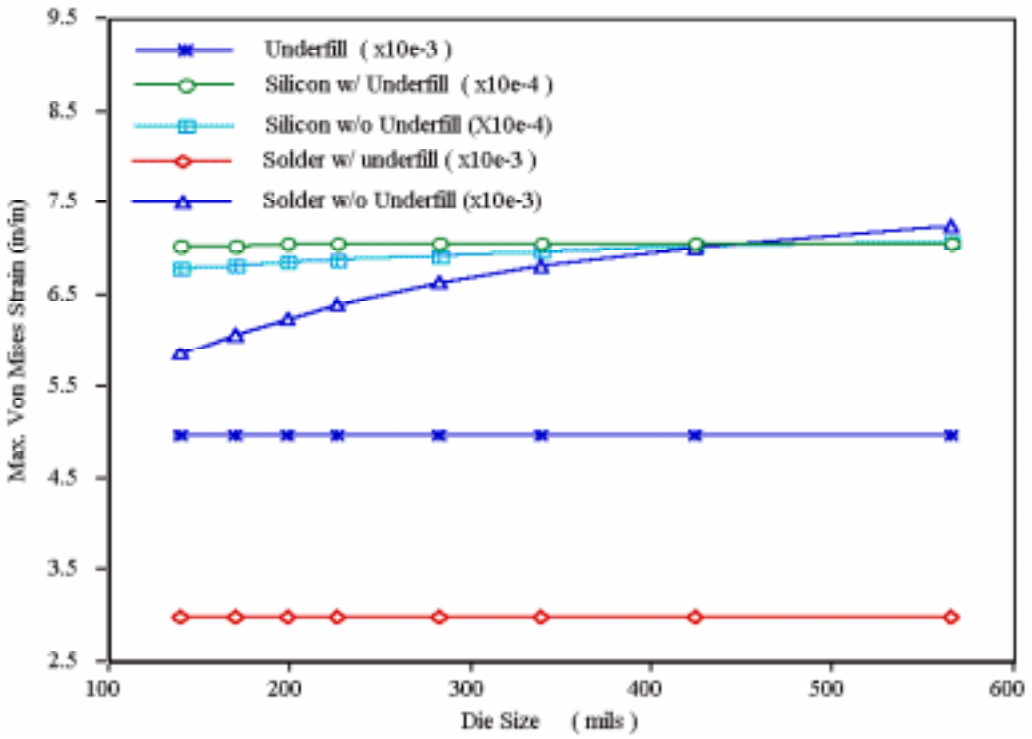


Figure 9.7 Parametric study results for die size

9.3.7 Underfill Fillet Profile

Three key parameters governing the profile geometry were investigated: fillet radius, fillet base length and fillet height (Figure 9.8). The results show that the fillet height is more critical than the other two parameters. As shown in Figure 8, the maximum die EEP increases significantly (55%) as the fillet height decreases. The under-

fill EEP, however, does not follow the same trend. It decreases by 21% over the height range studied. The solder joint EEP shows little movement. This prediction has been observed through an independent DOE study at Motorola [GIES94]. It has been found that the fillet base length and the fillet radius have minimum impact on the EEP (only approximately 3-5% strain variation) over the sufficiently large parameter ranges.

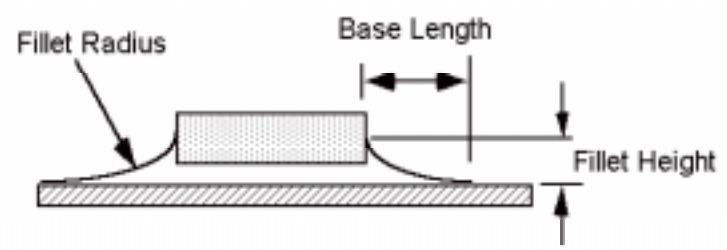


Figure 9.8 Key underfill fillet profile parameters.

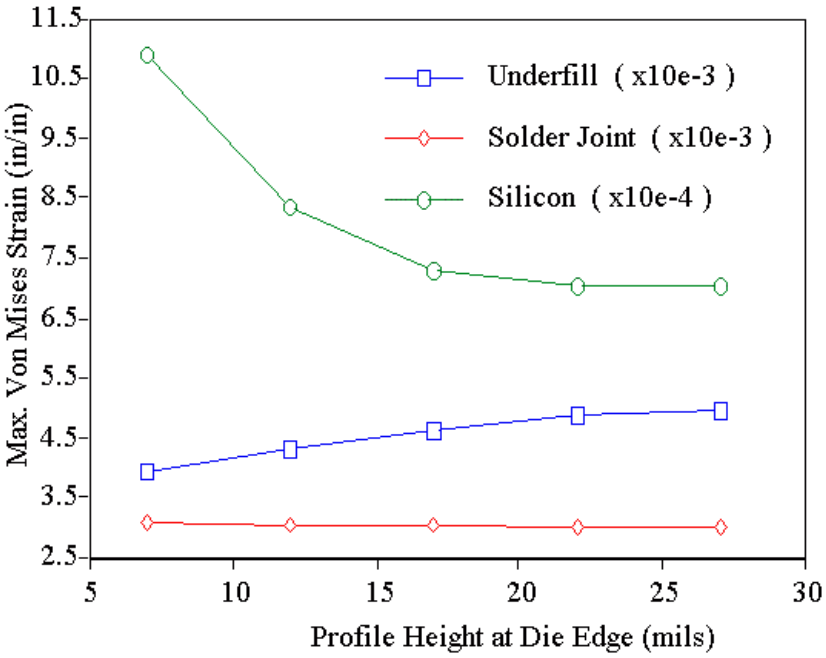


Figure 9.9 Parametric study results for underfill fillet height.

In addition, non-symmetric and no-fillet FCOB geometry are also analyzed as part of fillet parameters in the study (Figure 9.10). The results shows non-symmetric

fillets, on die edge side, has little impact on EEP result, compared to symmetric. But, study shows a significant EEP reduction by removing fillets. Note that the fillets in this study are built as a module, so it may easily be added or removed on both edges of the die. The non-symmetric fillets are created by changing parameters of base length, fillet height, or fillet radius.

9.3.8 Initial PWB Warpage

The initial bare PWB warpage, combined with various elevated temperature assembly processes, may often produce warped FCOB structures. This warpage is typically created by process induced residual stress. It will be of great interest to understand the reliability impact due to such warpage. A positive 75 ^{o}C temperature was applied to the models. As shown in Figure 9.11, the positive warpage (concave shape) will further worsen the reliability by adding as much as 25% additional strain to the that of the flat PWB case. In contrast, the convex initial warpage will alleviate the maximum EEP at a lesser degree (8%).

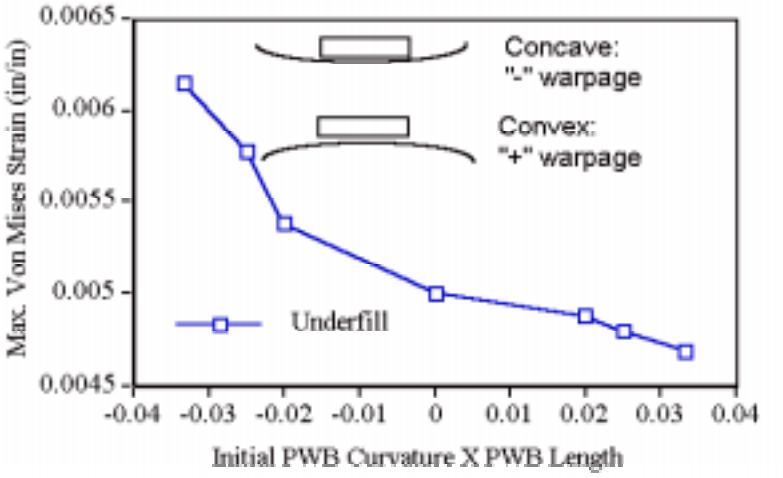


Figure 9.11 Parametric FEA results for initial warpage study

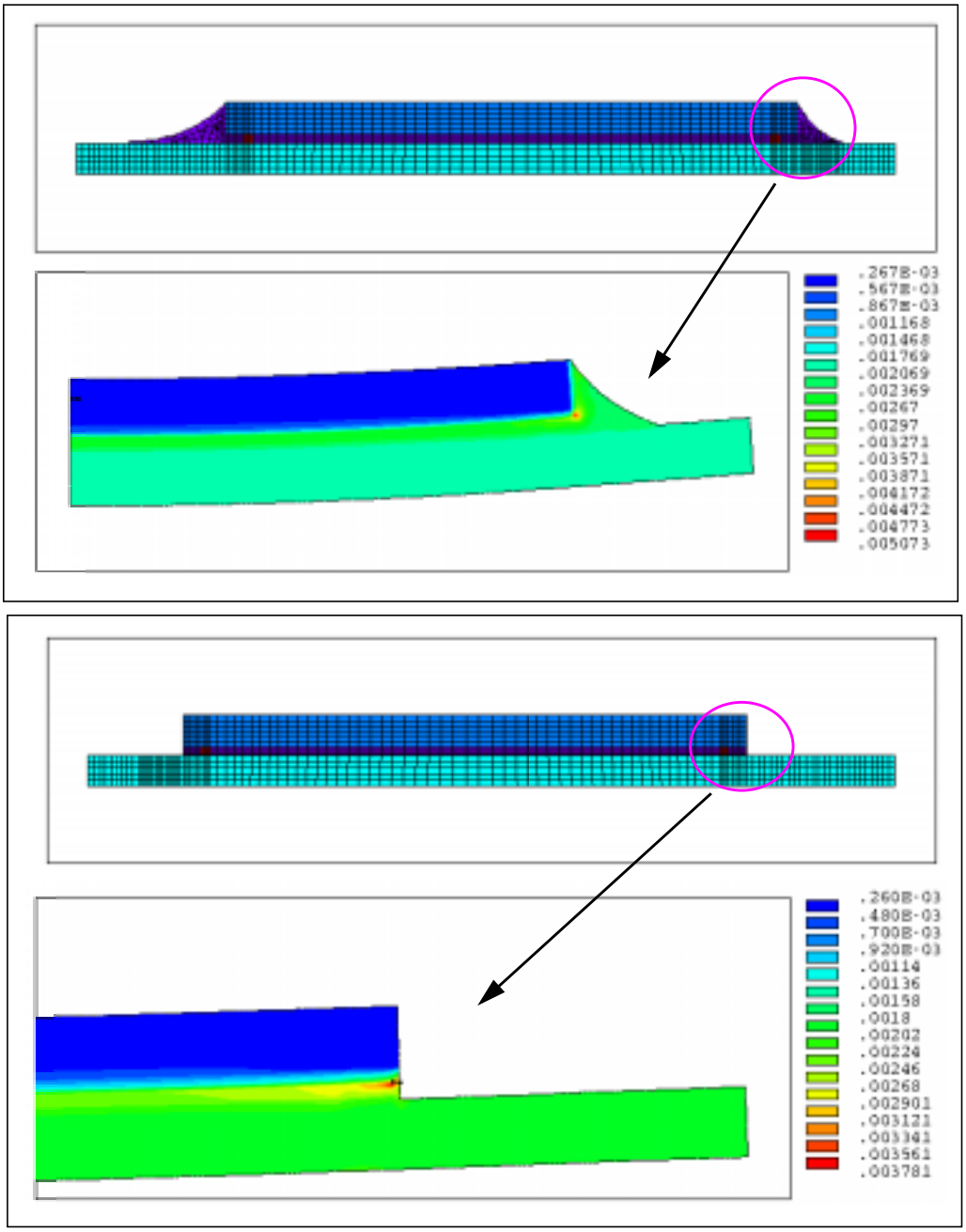


Figure 9.10 Parametric study for non-symmetric and no-fillet FCOB.

9.3.9 Material Properties

The CTE and the Young's modulus are the two most influential material properties in dictating the reliability of FCOB assemblies. Evidence also shows that these material properties of underfill and the PWB can vary significantly from vendor to vendor depending on the composition of the materials, the process conditions, or even storage environment. It is very useful to understand how the changes in material properties can affect the aforementioned failure mechanisms (Table 1). Figures 9.12 through 9.16 show the changes in maximum EEPs as different material properties vary between 80% and 120% of their baseline values. It is apparent that maximum EEPs become larger when the underfill CTE increases, although this trend for the underfill is more dramatic (32%) than those for the solder (3%) and the die (5%). In the case of the underfill Young's modulus study, the maximum EEPs for both the solder (1%) and the underfill (10%) dwindle and the EEP in the die (3%) increases as the Young's modulus of the underfill increases. In addition, increases in both the PWB CTE and Young's modulus will always cause the EEPs to increase. It seems that the PWB CTE has the most significant impact on the EEPs in the die and the underfill (37% and 18% respectively).

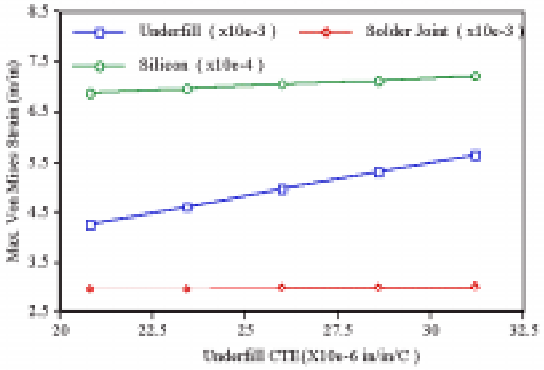


Figure 9.12 Parametric FEA results for underfill CTE

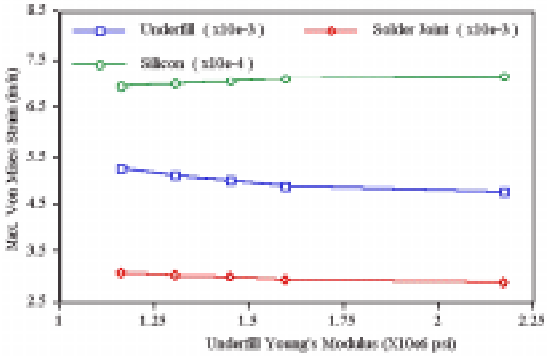


Figure 9.13 Parametric FEA results for underfill Young's modulus

9.3.10 2D Versus 3D Models

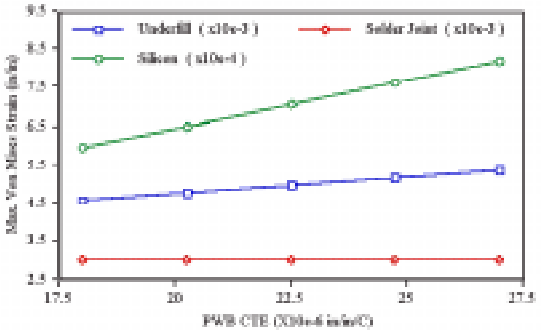


Figure 9.14: Parametric FEA results for PWB CTE.

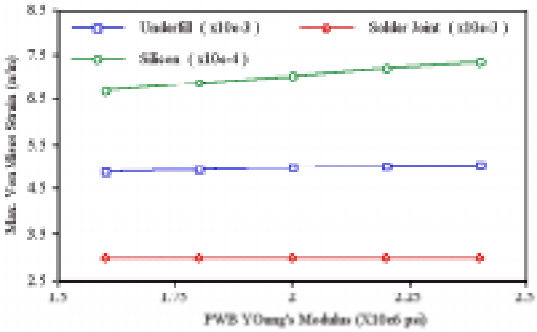


Figure 9.15 Parametric FEA results for PWB Young's modulus.

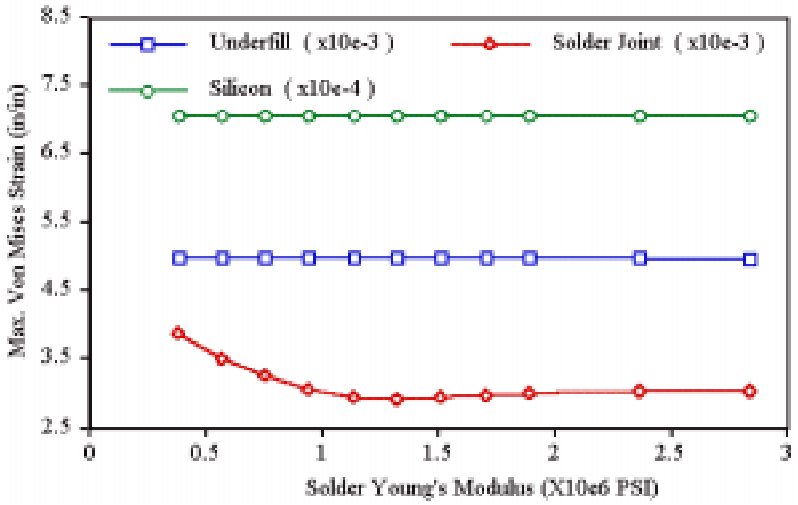


Figure 9.16 Parametric FEA results for PWB CTE.

To validate the aforementioned 2D models, 3D models were developed with an emphasis on geometric details especially for the solder joints. As shown in Figure 9.17, only a one-eighth of the assembly was modeled by MP/FEM. Figure 9.19 shows the parametric FEA results for the underfill thickness study for both the 2D and the 3D models. The results show that the 2D model underestimates the underfill and the die strains by as high as 73% and 23% respectively, but overestimates the solder EEP by 6%. It is suspected that these discrepancies are due to the 2D plane-strain assumption and the 3D

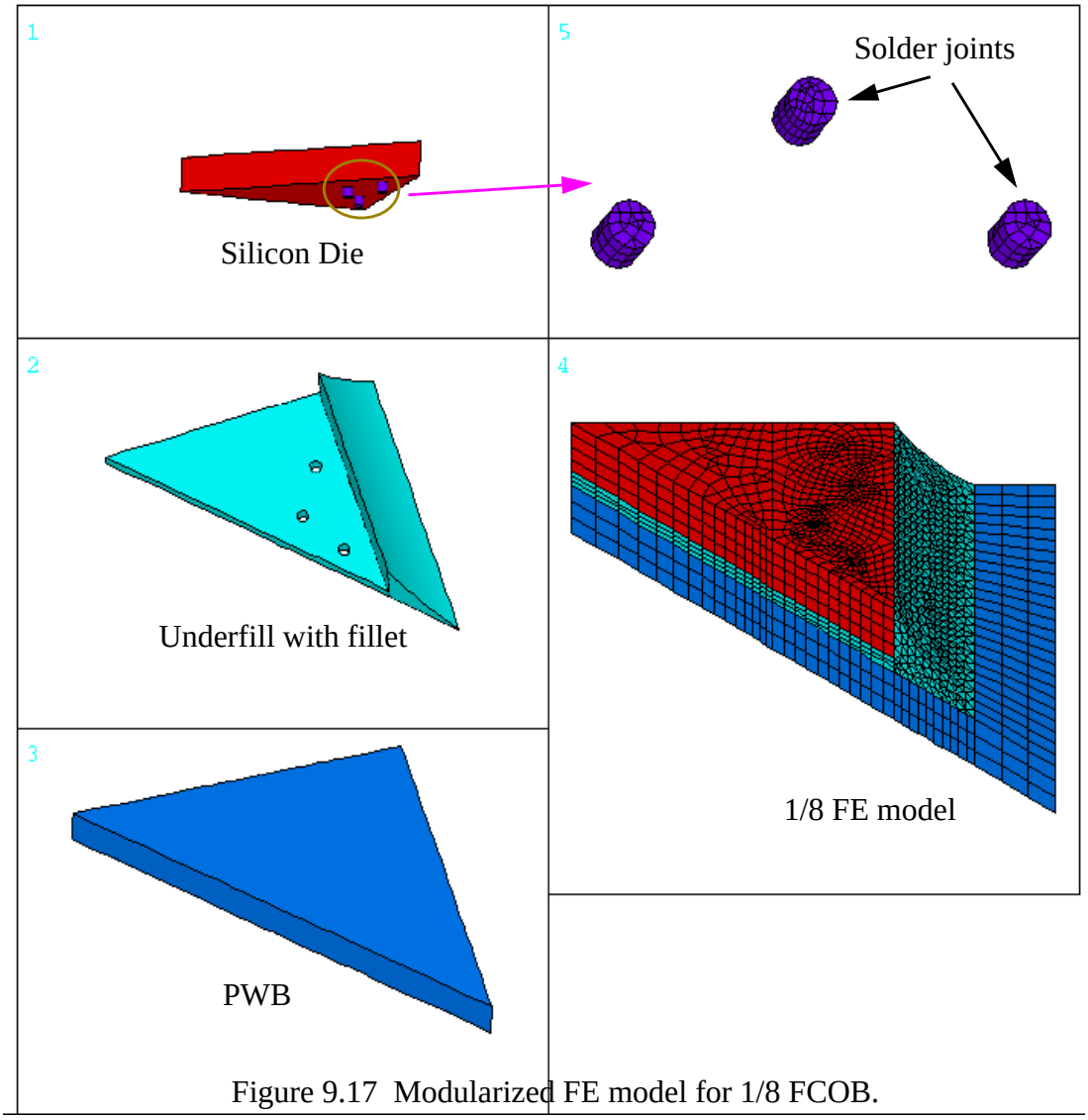
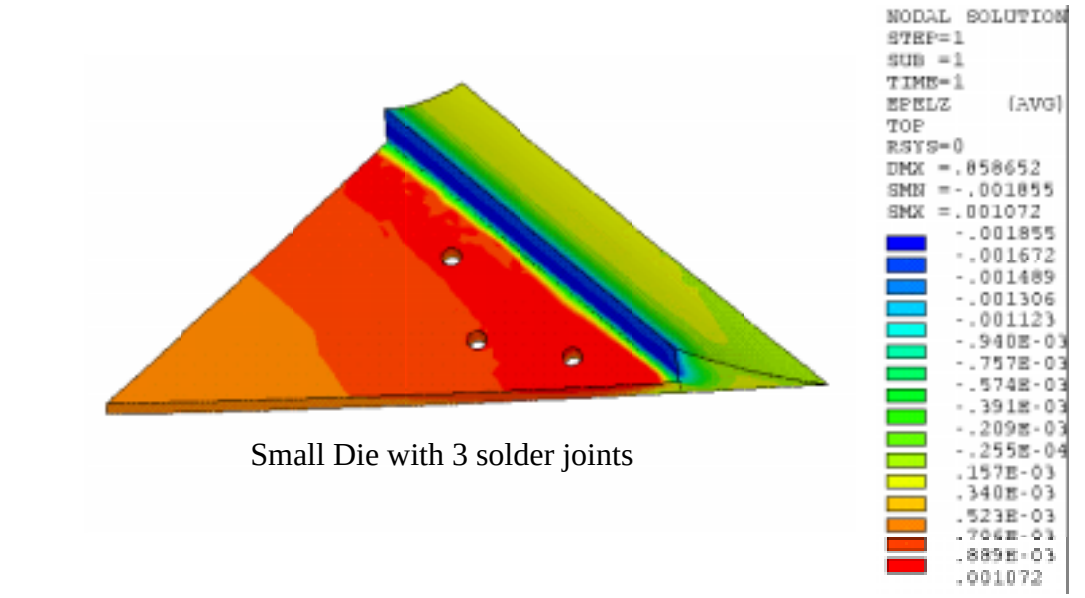


Figure 9.17 Modularized FE model for 1/8 FCOB.

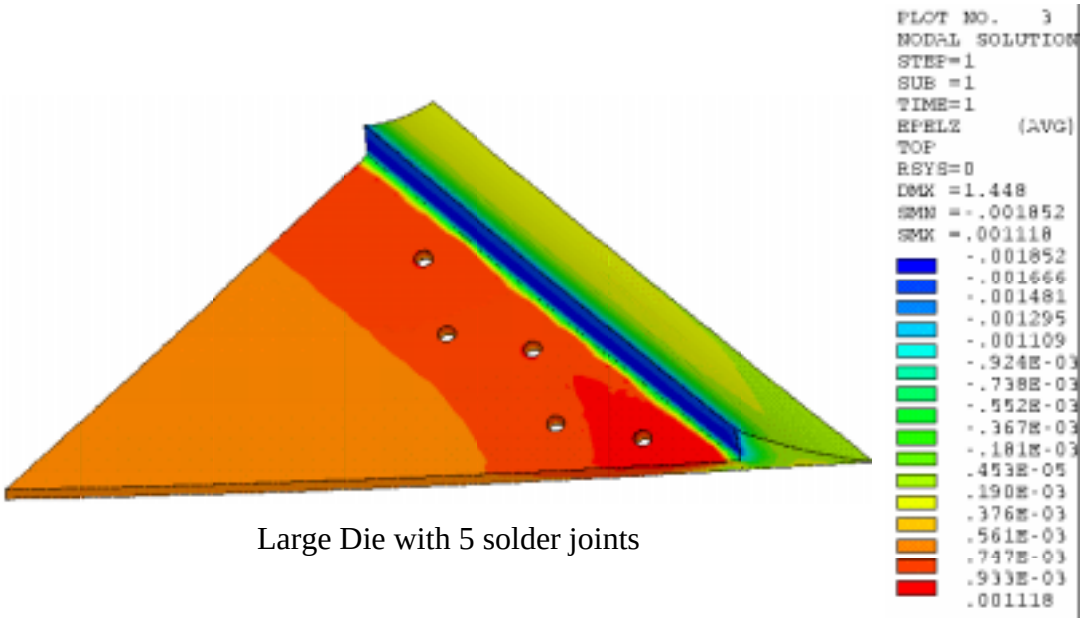
corner effects.

The sensitivity studies of die size and solder location are repeated in 3D FE model. Figure 9.18 shows EEP plot of two underfills. Top one is a small die with three solder joints, and another is a larger one with 5 solder joints. Though the EEP values in 3D are larger than that in 2D, the conclusions are similar. The EEP value are very sensitive to solder location, not to die size.

However, these over-/under- estimations are found to be very consistent for all



Small Die with 3 solder joints



Large Die with 5 solder joints

Figure 9.18 3D sensitivity studies of die size and solder location.

thickness studied. For the purpose of comparing various design options, 2D results are still qualitatively trustworthy and useful.

9.3.11 Design Optimization

Design optimization using ANSYS has been performed for minimizing the EEP

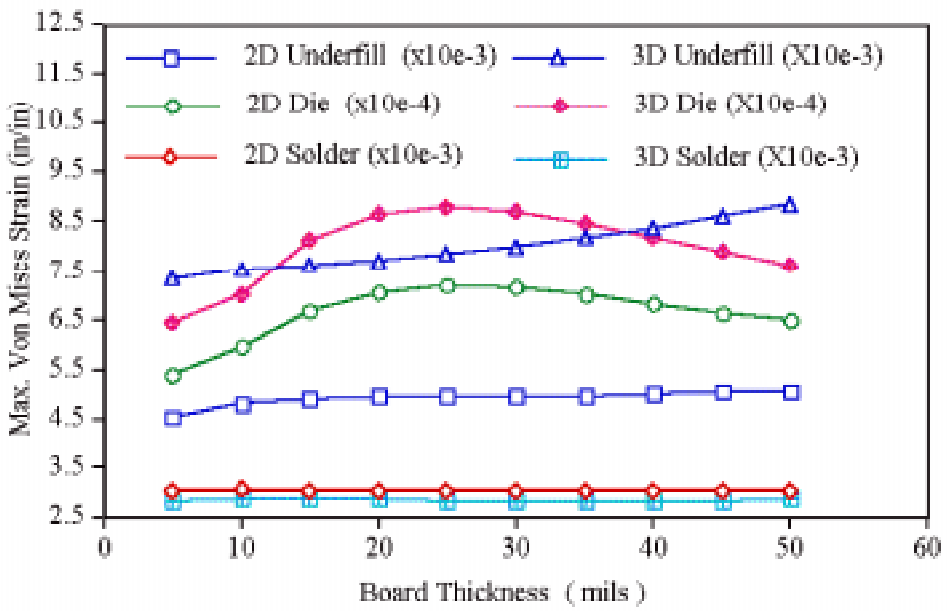


Figure 9.19 Parametric FEA result comparisons for 2D and 3D models.

in the die, the solder joint, and the PWB. Sequential Unconstrained Minimization Technique can be used in program code. As shown in Table 9.3, the PWB thickness, die thickness, and the underfill thickness were selected as the design variables because, from the previous analyses, it has been determined that they all have significant impact on the EEPs. Figure 9.20 shows the design optimization results for minimizing the underfill strain. It took ANSYS 15 tries to reach the goal. Depending on the criticality of different failure mechanism, the values of these design variables can vary. For instance, thinner PWB and die but thicker underfill can effectively minimize the maximum EEP in the underfill and the solder joint. On other hand, thinner die and underfill, coupled with medium thick PWB, are more desirable for reducing the EEP in the die.

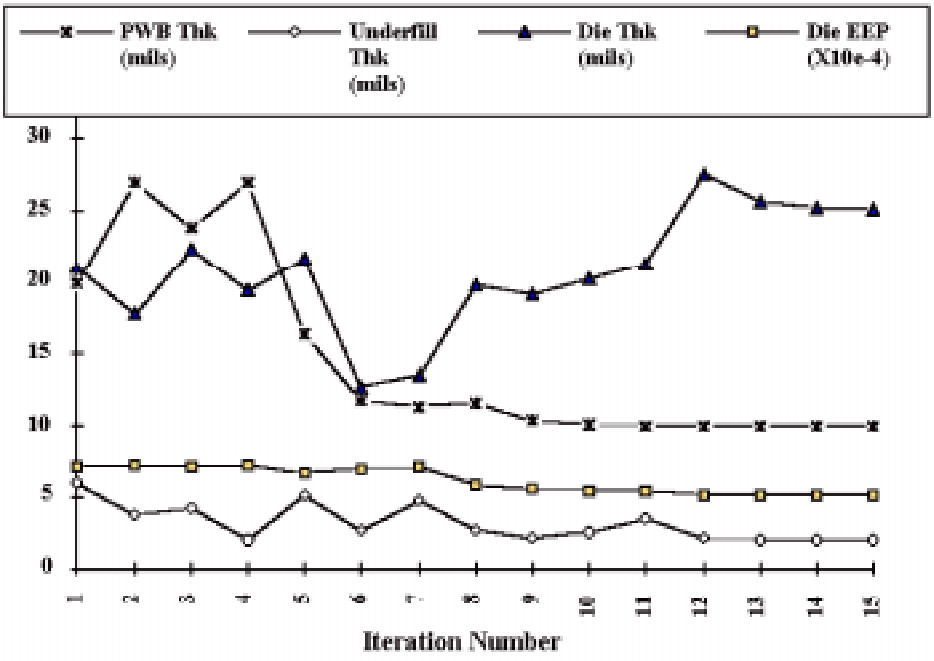


Figure 9.20 Design optimization for minimizing the die EEP

Table 9.3 Optimal designs for three case studies.

Case #	1	2	3
Design Variables	Die Thickness	Die Thickness	Die Thickness
	10 mils	13.5 mils	10 mils
	Undefill Thickness	Underfill Thickness	Underfill Thickness
	2 mils	6 mils	6 mils
	PWB Thickness	PWB Thickness	PWB Thickness
	25.2 mils	10 mils	10 mils
Objective Function	Die EEP	Underfill EEP	Solder EEP
	0.0051 in/in	0.00395 in/in	0.00286 in/in
# of iteration	15	14	14

9.4 Conclusions of Parametric Study

A comprehensive parametric finite element analysis for the flip chip on board (FCOB) structures has been conducted to investigate the reliability impact due to a number of selected design/process parameters. These parameters include die size, die thickness, PWB thickness, initial PWB warpage, and material properties. The results show that underfill CTE, die CTE, underfill fillet height, underfill thickness, die thickness, and underfill thickness can significantly affect the reliability of the FCOB structures studied. It has been illustrated in this study that optimal design parameters are attainable using finite element based design optimization algorithms. In addition, the strain evolution at the cool-down and the heat-up stages during the thermal shock testing was also analyzed. Some key results have been validated through available experimental data published elsewhere. It has been concluded that the parametric FEA technique is a very cost-effective and vital tool in evaluating the reliability of FCOB assemblies. The analysis results can be used to generate a useful set of assembly design guidelines.

Chapter 10

Case study 2

MP/FEM for product Board-level thermomechanical analysis

Determination of the thermo-mechanical behavior of an electronic product at board-level, not just at component level, becomes increasingly important design aspect in an electronic product design process. In order to create this design analysis capability, MP/FEM approach is used to rapidly generate a mechanical FE model, and perform thermal, mechanical bending and vibrational (modal) analysis. This is the first model ever built, in the literature, to allow a designer to perform mechanical analyses at system level.

10.1 Introduction

Up to date, most thermo-mechanical models, for especially for electronic products, are developed for either a single connection or a single component. All joint connections of a component are treated same, and the impact from its neighboring components are ignored. These isolated models are used to study the mechanical behaviors and the failure mechanisms of a critical joint or component. Since the components and joint connections in these electronic products are relatively apart, these models are

valid, and provide reasonably good results. However, due to the recent advance of electronic packaging technology, significant improvements have been made on the density and size in new electronic products. Decreased component size and pitch lines create strong interferences among all components and their joint connections. A mechanical study, based on an isolated model, may no longer be valid. A component may show different mechanical behaviors in system level than by itself alone. This requires that a thermo-mechanical study has to be conducted on an entire system level. Unfortunately, there is no effective and practical modeling method can be applied for developing a model of a populated PWB.

Mechanical reliability analysis of an electronic packaging product are generally performed by a mechanical expert only after electrical design. In addition, mechanical model (finite element model) building phase generally require 80~90% of total analysis time. These limitations require new modeling methodology has to be developed.

To respond to the growing needs of mechanical modeling and the simulation in electronic design process, the developed approach, Modularized & Parametric Modeling Methodology (MPFEM), can be used to perform rapid board level thermomechanical analysis. In this chapter, an example is given to show how to use MP/FEM to generate a board-level finite element model.

10.2 Case description

A populated board with SMT components is used as an example for this case study. The populated board, used in this study, is provided by a member company of MaRC. The objective of this study is to show the capability and flexibility of MP/FEM. Since the most time-consuming and critical part of a mechanical analysis is to build an appropriate FE model, the emphasis of this study is placed on the model generation and modification. Thermal, mechanical bending, and vibrational (mode) analysis are

performed upon the developed model.

10.2.1 Failure mechanisms

Because of the packaging miniaturization, components and interconnections are become more and more close to each other, an isolated mechanical model can no longer determine its mechanical characteristics. An isolated component, with good reliability performance, may show failures, when it is mounted onto a board with other components. Furthermore, some failure mechanisms can be attribute to all the components on the board. Without a complete model, which includes all the components, the thermo-mechanical study may not discover the true failure mechanism. There are a few observed mechanical failure mechanisms that can be only studied on a board-level mechanical FE model:

warpage. During both manufacturing process and material handling process, the board warpage may be developed. The warpage may be caused by FR4 board itself, components deformations, non-uniform temperature loadings, and external forces and bending. These factors may be combined to cause more serious warpage problem. This warpage problem may only be found after all components have been mounted on the board.

Solder Joint crack. When a PWB is subjected to external forces, such button push and shock impact, a solder joint of a component may be cracked by excessive deformation. The deflection, or the stiffness of a board, is determined by overall components and the board. The questions, such as which solder joint, or which component, is going to be vulnerable, can not be answered without a board-level analysis.

Delamination and solder joint fatigue. Similar to solder joint crack problem, a solder joint may be failed due to the delamination of a structure, or due to solder fatigue. Compared to the solder joint crack problem, this one is considered to be more moder-

ated, and needs more loading cycles to show a failure.

Hot spot. The temperature distribution on a board is dependent on all the components on a board. It is determined by component geographic locations, heat generation power of each component, and heat removing pass.

Vibrational and bending Problem. When a PWB is mounted on a moving vehicle, such as automobiles or missiles, the vibration may cause board deflect, and exert stresses on the solder joints of components. To identify the joint that may cause failure needs board level consideration. Similarly, during manufacturing handling and/or assembly process, a joint may be damaged when a PWB is subjected to a bending force, such as depanalization.

10.2.2 Modeling assumption

In order to perform the model solution in a simple manner, the following assumptions are made for this study:

1. The geometry of the board is de-featured. De-featuring implies that lots of small features are ignored, such as small screws, notches, holes. The board is assumed to have a rectangular shape. Only desired components and joints are presented on the board.

2. The board is flat. This assumes that no initial warpage is considered in the modeling and solution process.

3. As no mechanical models has been developed for vias, the board is assumed to have no vias.

4. The board is uniform board. Due to the lack of copper trace distribution and board layout geometry, the board is considered as an uniform board.

5. in global analysis, linear material properties are used. As more detailed analysis is performed in local analysis, global analysis is regarded as first pass of solution.

6. In component library, it is assumed that the library only contains the compo-

nents used for this study. Since this study is to demonstrate the concept of MP/FEM approach, only a few components are picked, and placed into the library.

7. In global analysis, no solder joints are placed under silicon dies in DCAs. This is because the silicon is coupled with the PWB by encapsulant, and the silicon is much more stiff than the PWB and solder. More detailed solder joint analysis may be performed in local analysis, as showed in Chapter 9.

8. The geometric size of components and solder joints do not reflect real product geometry. The geometric data have been modified.

9. The components and their lead frames are assumed to be perfectly aligned and planar, with respect to the PWB.

10.2.3 Components description

The PWB contains 13 components, which includes: (1) 2 DCA, one has a squared silicon die, another with a slim rectangle; (2) 2 TSOP with gull lead, one has a squared package with 4 side lead, another has a narrow rectangle with 2 side leads; (3) 1 TSOPs with J lead, it has a square package with many leads on 4 side. (4) 6 Passive components with 2 side solder joints. (5) 2 Passive component with 3 solder joints.

The parameters used for the TSOP with J-lead is listed in table 10.1. The geometric data for other components can be found in appendix I.

Table 10.1 Parameters for a TSOP component with J lead

MGP	Attribute	value (mils)
	Lead side	4
Component Body	lead width	12
	margin x	18
	margin y	18
	No of lead (x)	10
	No. of lead (y)	10
	lead separation (x)	12
	lead separation (y)	12
	body thickness	21
J-Lead	lead shoulder	6
	RC of shoulder	4
	lead vertical height	8
	RC of base	4
Solder Joint of a J-lead	solder outer extension	3
	solder inner extension	4
	solder thickness	2.5

10.3 FE model generation

In this section, a board-level FE model will be generated by MP/FEM. Since the detail procedures and algorithms have been introduced in Chapter 6 and 7, only brief steps are presented in the following sections. The components are selected from a pre-defined library. The assembly process is based on a CMAT tree, which is created for the

populated PWB. The material properties are stored in a file. The value of material properties are copied from SINDAS measurement database.

10.3.1. Component library Creation

The first step of a component library generation is to define a component list. In this case, four different types of component are defined: TSOP with gull lead; TSOP with J-lead; DCA; and passive components. For each component, it consists of several MGP modules. For example a TSOP with Gull lead is composed of different MGP modules (Figure 10.1): Plastic body, Gull lead, solder joint and a piece of PWB board (simplified module). Each type of the component is described in a file, which is written in C and ANSYS script language. (See appendix II)

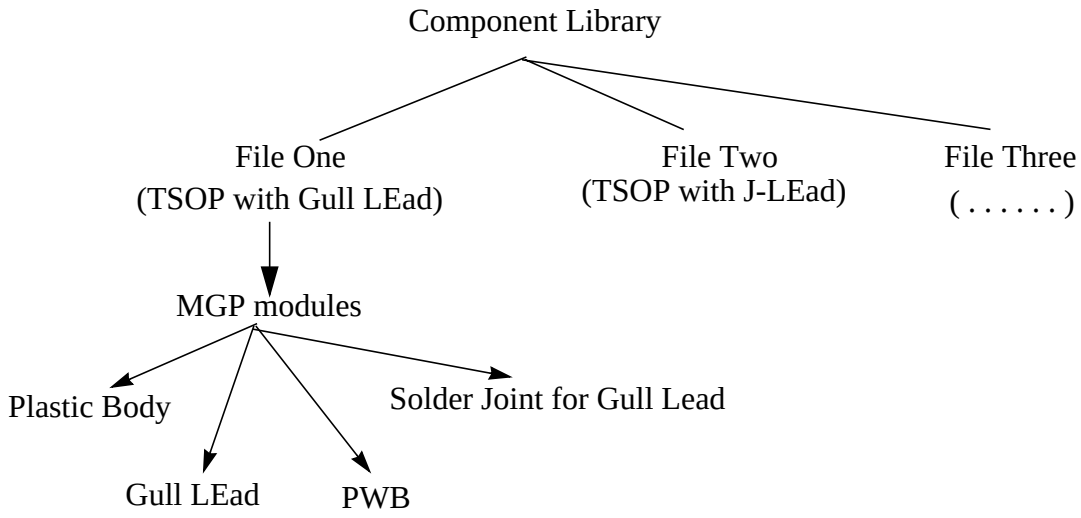


Figure 10.1 Component file configuration.

Since each component is a complex assembly of different geometry and materials, one must decide how much details of a geometry and what type of mesh control parameters to be included for a finite element model. Each model of a component has to

be built flexibly, such that its geometry and mesh grid may be easily modified without knowing detail of finite element modeling technique. Geometry data and analysis type are the only information needed to create a finite element model. This generated model is immediately ready for either calculation or assembly (onto a PWB). Thus, an automatic link, which constrains the geometry and mesh control for a required analysis, has to be defined in each mechanical component module. Similarly, the analysis capabilities, such as what types of analysis and loads to consider, have to be determined in the model building phase.

The key of a model creation is using parametric representation. Each physical data or modeling step of a component are defined and/or recorded by predefined parameters. These parameters are classified into a few categories, such as parameters for geometry, material, analysis type, mesh control, and component-to-component relation. Each parameter is linked and/or constrained internally by other parameters, or externally by the parameters of neighboring component. The definitions of parameter categories for a TSOP component has been showed in Chapter 7. The parameter definitions for rest of components are listed in Appendix III.

It is important to note that the development of a mechanical model library can be updated at any stage of modeling process. The library functions as an expert system, which saved FE modeling experiences for different types of component. Development of a good library requiring the knowledge about many factors, which may be limited by a single person.

An electrical designer may specify a component and its location, and then create a FE model for analysis. However, when a component model is called for assembly, a user has to know what parameters required to complete a global model. Some of these may be asked by program, others may be linked to other resources, or be specified as default values. In order to fully integrate this modeling methodology into an ECAD system to achieve automatically analysis capability, a standard data structure has to be developed.

Development of the data structure is primarily used for the interface of ECAD system. This aspect has not yet been studied.

10.3.2 MGP module testing

Each developed MGP module has to be tested before it is saved into a library. The purpose is to check the setting of meshing parameters for the mesh generation. Since the quality of a solution is dependent on the mesh pattern and mesh density, it is important to confirm that the meshing control parameters can be flexibly adjusted. The following items have been checked for each MGP:

1. Element aspect ratio. Highly distorted elements at critical area can not produce good results. When aspect ratio of a element becomes more than 6, the result of that element may be questioned. The aspect ratio of an element can be adjusted by adding more element divisions in the distorted direction.

2. Meshing pattern. The meshing pattern of a MGP may be mapped mesh, triangular mesh, or combination of the two. During certain conditions, requested mesh pattern may be failed. For example, the mesh control parameters, which is set for two jointed lines with an angle of less than 90^{o}, can not produce elements, when the angle become close to 180^{o}, as the two lines turn into one straight line.

3. Solution convergence. Since the FEA is an approximation method, the obtained results have to be checked for a convergence. The convergence of a MGP model implies that, as the size of an element is continuously reduced, a converged result can be obtained. Though the model result may not have been converged at the checking time, but it should show the trend of convergence. Sometime, a model may show a significant result variation, or divergence.

4. Element size reduction. The reduction of the element size is often used when convergence criteria is not achieved. It is an important mesh modification method. In

the module testing step, the element size of each module are reduced to 1/2 and 1/4 of the original size.

5. Element mid node creation. Similar to element size reduction, adding mid nodes to an element is another version of mesh modification. Addition of the mid nodes to MGP modules are tested.

10.3.3. CMAT tree development

As described in Chapter 6, a graph tree of CMAT has to be customized for each product configuration. The tree is object oriented, and contains the geometric hierarchy information for product decomposition. The G_{CMAT} for this case example is given in Figure 10.2.

The root of the tree is the starting point, which represent the entire product in this case study. Since the root has only one PWB, it has only one child. There are 13 components listed under the PWB node. The two passive component type are showed as one component node, as they are the same. The MGP lists of the second DCA and TSOP with gull lead are skipped, since they are similar to their first one.

10.3.4. FE model assembly

Once the G_{cmat} is constructed, the assembly sequences and procedures can be generated by using DSF algorithm, described in Chapter 6. The components are placed onto the board by this assembly sequence, one at a time. The detailed steps of how to generate this sequence can be found in section 6.5. The results, by using G_{CMAT} to assembly a board-level model, are presented as follows:

First, a DCA is placed on the lower left corner of a board, as seen in Figure 10.3. The DCA has a squared silicon die. As seen on the picture, the DCA is a meshed model. The geometry and mesh density are determined by the imported data file (see

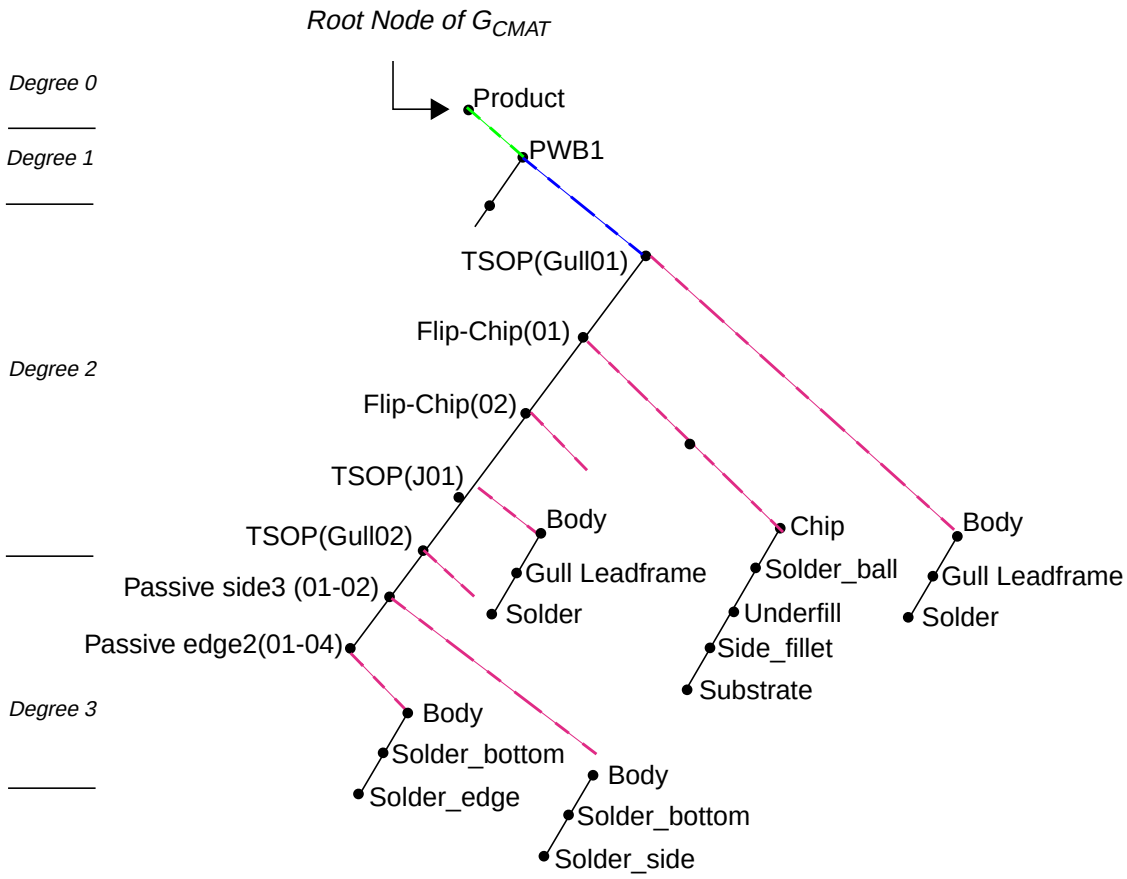


Figure 10.2 Construction of a CMAT for the PWB.

chapter 7 for detail). Followed by this component, more components are continuously placed onto the board, as seen in Figure 10.4. They are one TSOP with gull leads on four sides; one TSOP with J-lead on four sides; and two small passive components with 3 solder joints on sides. Notice that one passive component is placed horizontally, while another is place vertically. This can be easily achieved by specifying the angle of rotation as 90^{o} with respect to another.

The entire model is completed by placing rest of components onto the board. Eight more components are mounted onto the board: 4 small passive components with

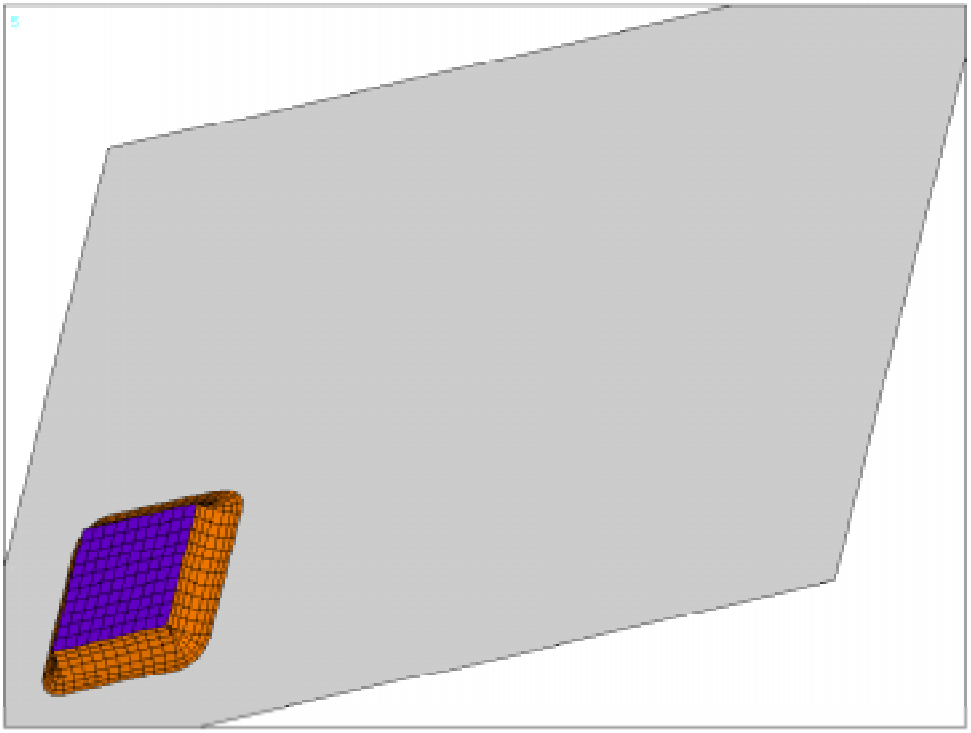


Figure 10.3 Placement of the first component on a bare board.

solder joints on edge side; 2 large passive components with solder joints on edge side; one TSOP with gull lead with two side lead frame; and one DCA with a slim rectangular silicon die. The new DCA, on the top-right corner, is basically duplicated from the previous DCA on lower-left corner, but different in the geometry size. As geometry sized changed, the meshing element number changed correspondingly, to keep the same mesh density. Similar to the duplication of a DCA, the new placed TSOP with gull leads on two sides is created by changing the value of module parameter, LEADSIDE, from 4 to 2. Figure 10.5 shows a board-level model with all the components, but without the mesh of the board. A enlarged TSOP corner part is also showed for mesh detail. Figure 10.6 shows a completed FE model for the entire board. The mesh of the board is based on the pattern of the mounted components.

As each component is relative independent to others, they can be treated as an

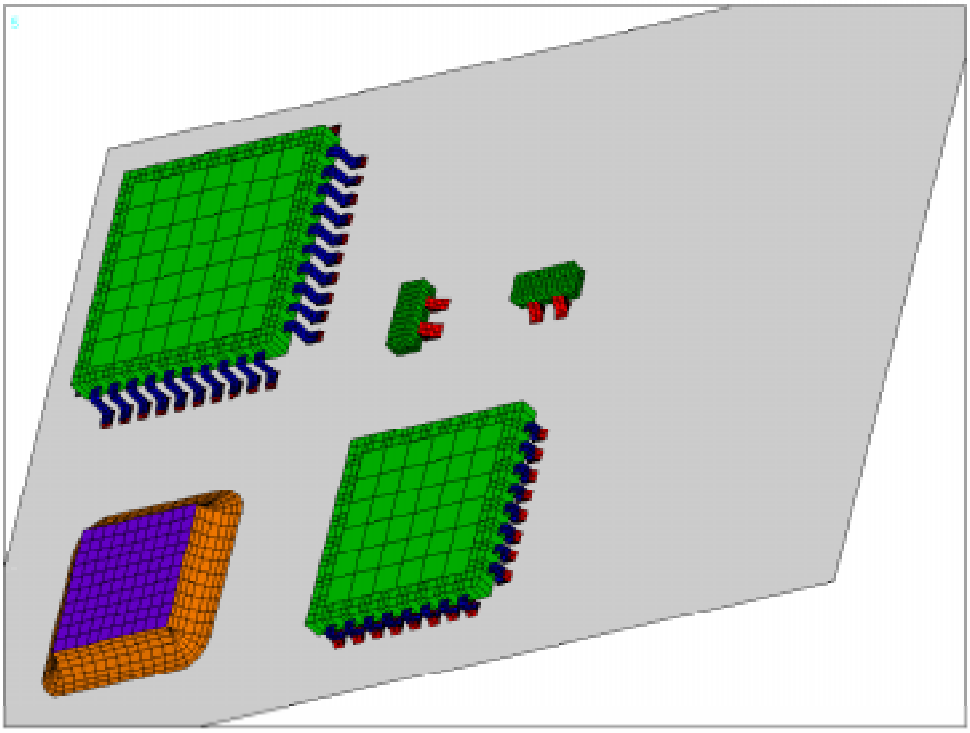


Figure 10.4 Four components are generated after a DCA placement.

"icon". They can be moved, or rotated, if necessary. The movement, or rotation operations, after the board mesh, can not be simply performed on the components, since the meshing pattern of the board has to be changed as well. The rotation operation can be achieved by deleting the board mesh and component first, then followed by the new placement of a component with modified geometric data. Figure 10.7 shows the new FE model that both TSOP and DCA are rotated. After rotation operations, the board mesh can be re-generated, based on the components orientations (Figure 10.8). The capability of these type operations are very important to concurrent mechanical designs in a product design process. As a designer may change the location and orientation of a component during the design process, it is essential that the mechanical model can be changed flexibly and simultaneously.

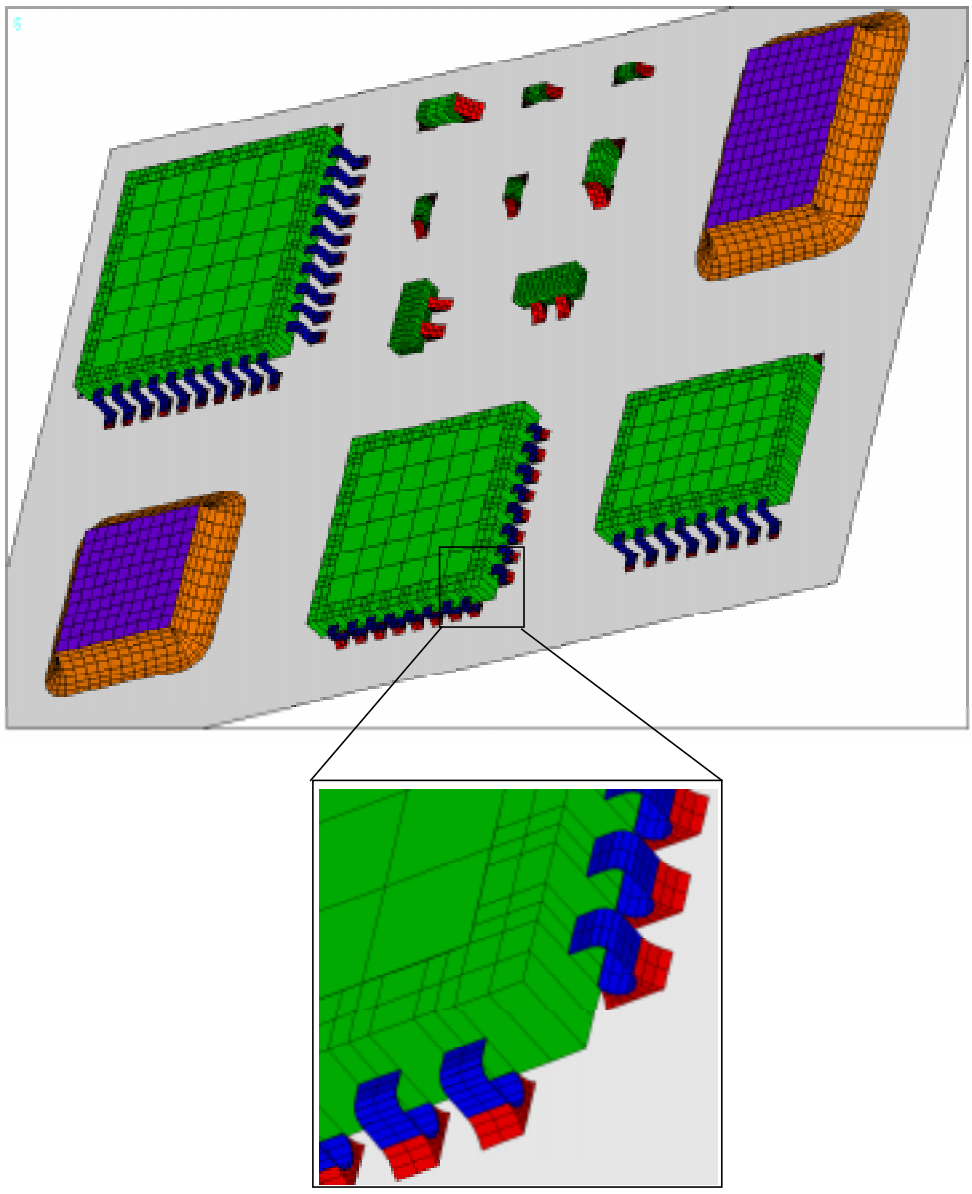


Figure 10.5 FE model for the components on the board.

10.3.5 Material library

The material properties for the materials used in this case study are saved in a file. The file serves as a material library. The material properties are sorted by material names. When the name is called from the MGP assembly program, the value of the

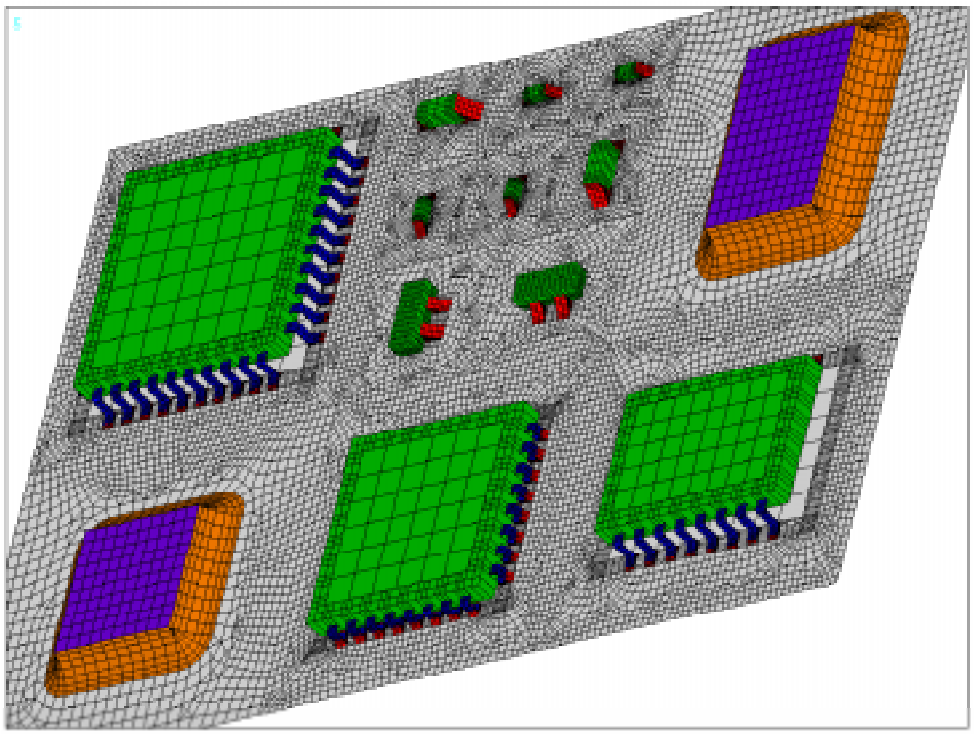


Figure 10.6 Completed FE model for the board and components.

material property is copied into that program. Thus, the material property for each MGP does not have to be defined until the final solution pass. In the case that a designer wants to look at another alternative material, he only needs to change the name of a material for that MGP. The linkage is automatic, and is implemented by a link-list structure in the C program. A few sample materials are listed in Table 10.2:

10.4 FE model Solution

The solution phase is giving a FE model to a finite-element-solver for evaluating results. The developed board-level FE model is used to conduct different types and different levels of analyses. Thermal, mechanic bending, and vibrational analyses are performed. Based on the coarse solution (global analysis) of a thermal study, more

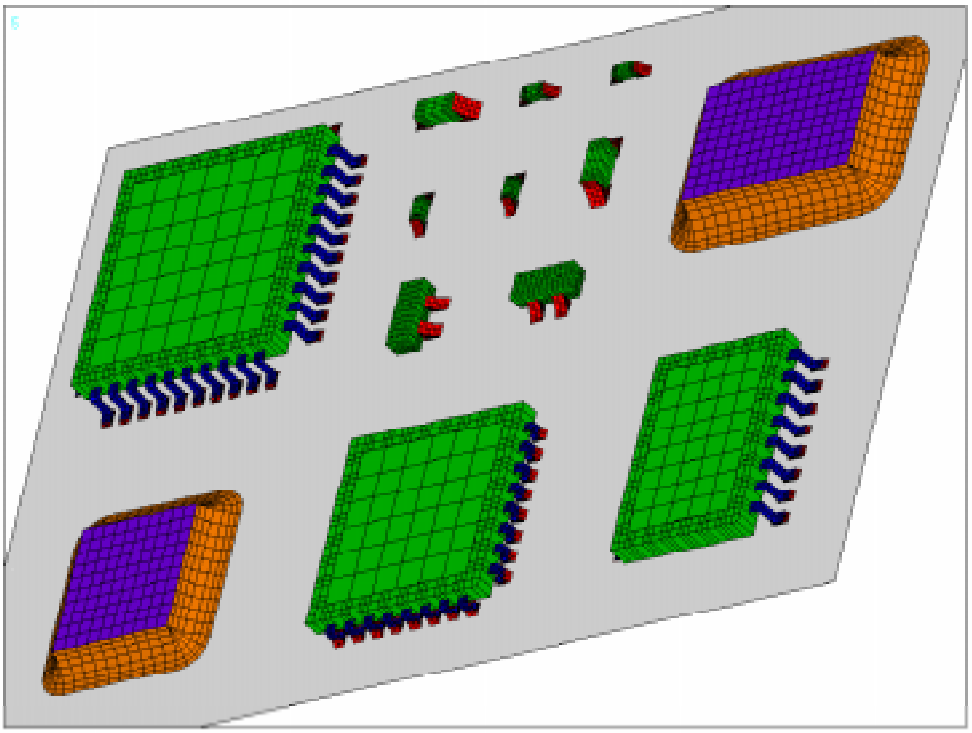


Figure 10.7 Modified FE model with rotated DCA and TSOP.

detailed (local) analysis are performed.

10.4.1 Solution preparation

The defined material properties and element types are automatically linked to a material database and an element library, respectively. Numerical value of each material is translated to the format required by ANSYS software before the start of a solution. The element default is choosing the element with lowest shape function in its class. After the first calculation is done, the second iteration will automatically performed to check convergence. In the second calculation, the element density or element order are improved, which could result in a longer solution time. In the case of non-convergence, the model may be refined by either h-version or p-version elements. Analysis types can be switched from one to another by simply changing the parameters of

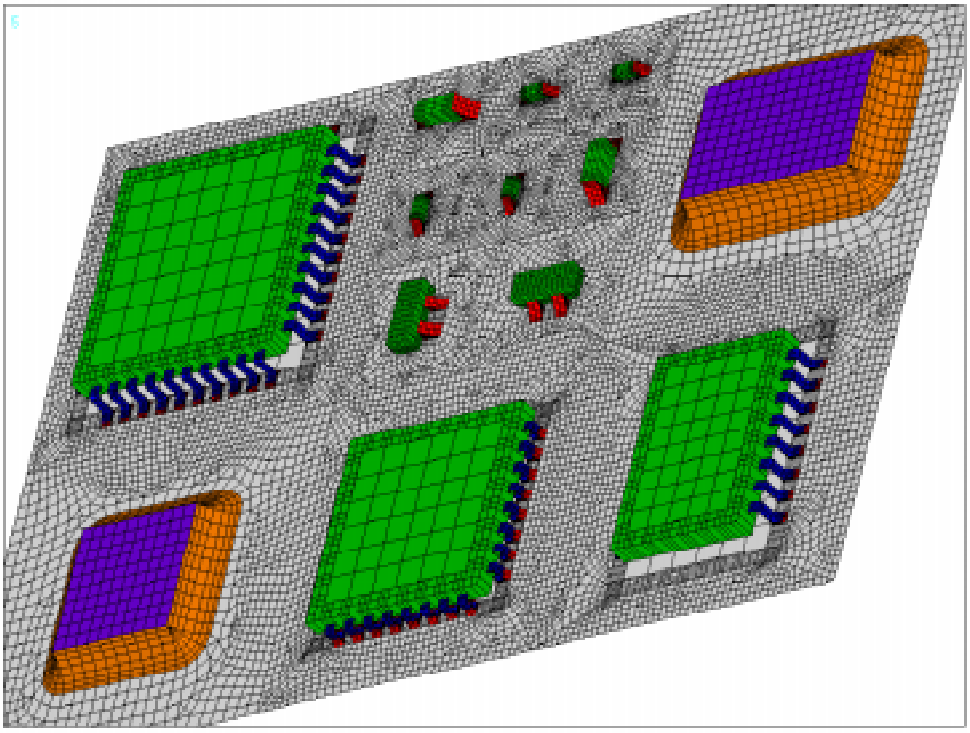


FIgure 10.8 Re-mesh model after components rotation.

Analysis_Type_Indicator(ATI). Once the ATI value is changed, element type, constrain equation, time step, and DOF output will automatically changed correspondingly. For each analysis, boundary condition and loading condition may be vary upon different applications.

As a global analysis, thermal, mechanical bending, and vibrational analysis are performed. The results are presented below.

10.4.2 Thermal Analysis - Global

The thermal analysis is to simulate the power switching process. The process assumes that all the components have a room temperature at the initial state. When the power switch is turned on, the components start to be heated up. Because of the temperature loadings, the stresses are created in components and solder joints. For simplicity, all active components are assumed to have the same power of 2W. The board

is assumed to be nearly isolated from the environment, as if it is enclosed in a case. Since it is a free convection and the heat removing capability is small, the heat dissipation is modeled as conduction. The room temperature is assumed to be 20^{o}C. The solution is done at the state when the whole assembly has reached a steady state temperature. The left side of the board is clamped, as the board is slided into a board slot.

Due to the CTE mismatch, the board is warped at the free edge. The wrapped shape is plotted in Figure 10.9. The strain distribution of the entire board is shown in

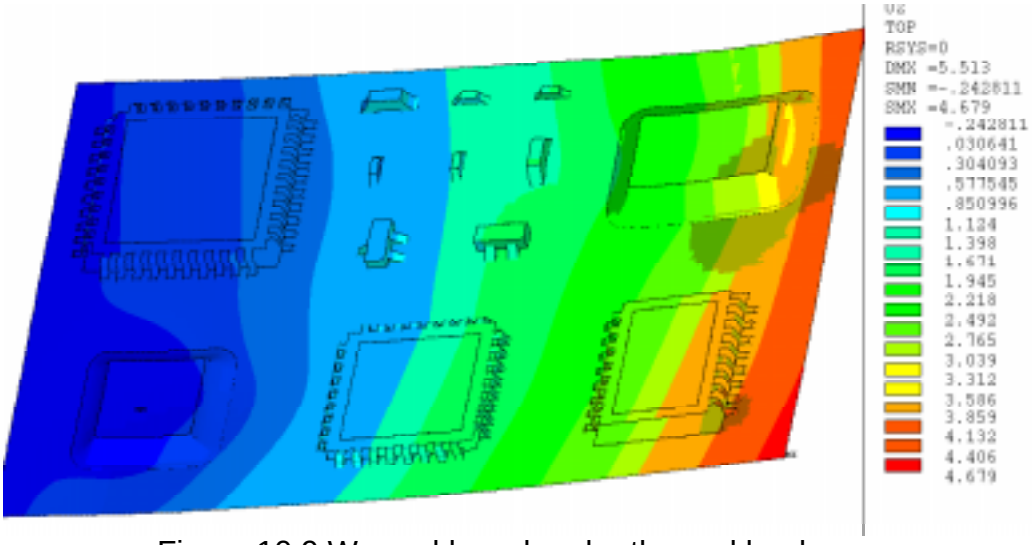


Figure 10.9 Warped board under thermal load.

Figure 10.10. From Figure 10.10, it shows the maximum stress on the board is around the underfill of the DCAs. This is because the epoxy couples the silicon die, with low CTE, to the board, with high CTE. The epoxy bonding prevents the solder joints underneath the die being stretched from the thermal stress. Since the solder joints under the DCA are protected by epoxy underfill, their stress and strain values are about the same as that of the underfill. Because of this, they are not presented in this case study. More detailed DCA solder joint studies can be found in Chapter 9.

One important aspect of the global study is to show the “worst joint connection”,

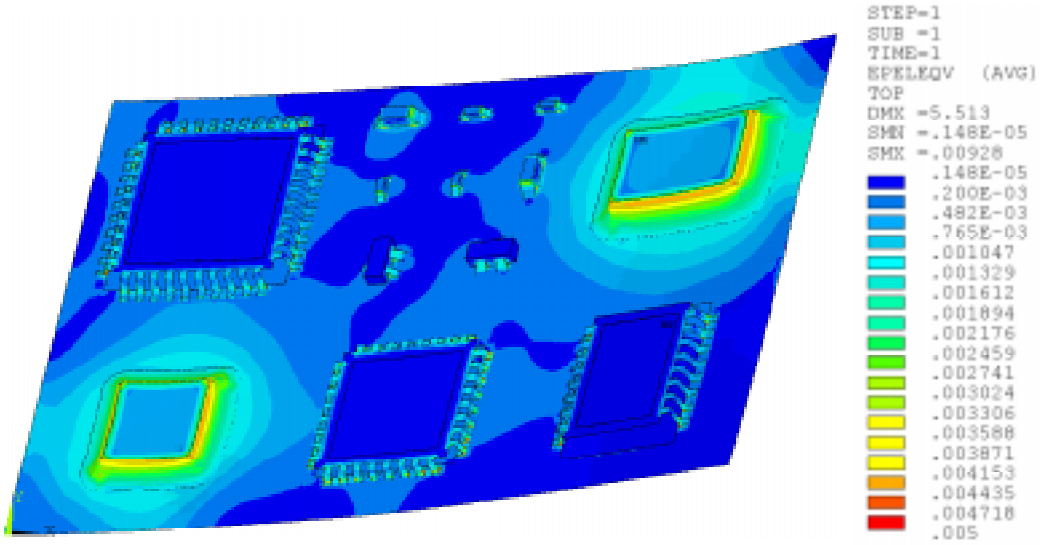


Figure 10.10 Strain distribution of the entire board under thermal load.

which is more vulnerable, compared to others. In Figure 10.11(a), it plotted all the solder joints for SMT components. The stress value of all the solder joints are sorted in the solution process. The joint, with highest stress, is marked by "MX" above the solder joint of a TSOP. (the word "MX" may be too small to see in this plot.) The maximum equivalent strain value for this solder joint is found to be 0.92%. The stress may not represent the real value. However, Since all the solder joints are calculated under the same assumption, they have about the same percentage of error, if they have. Thus, by looking this plot, it indeed indicates, under this specific thermal load, the J-lead joint should fail first.

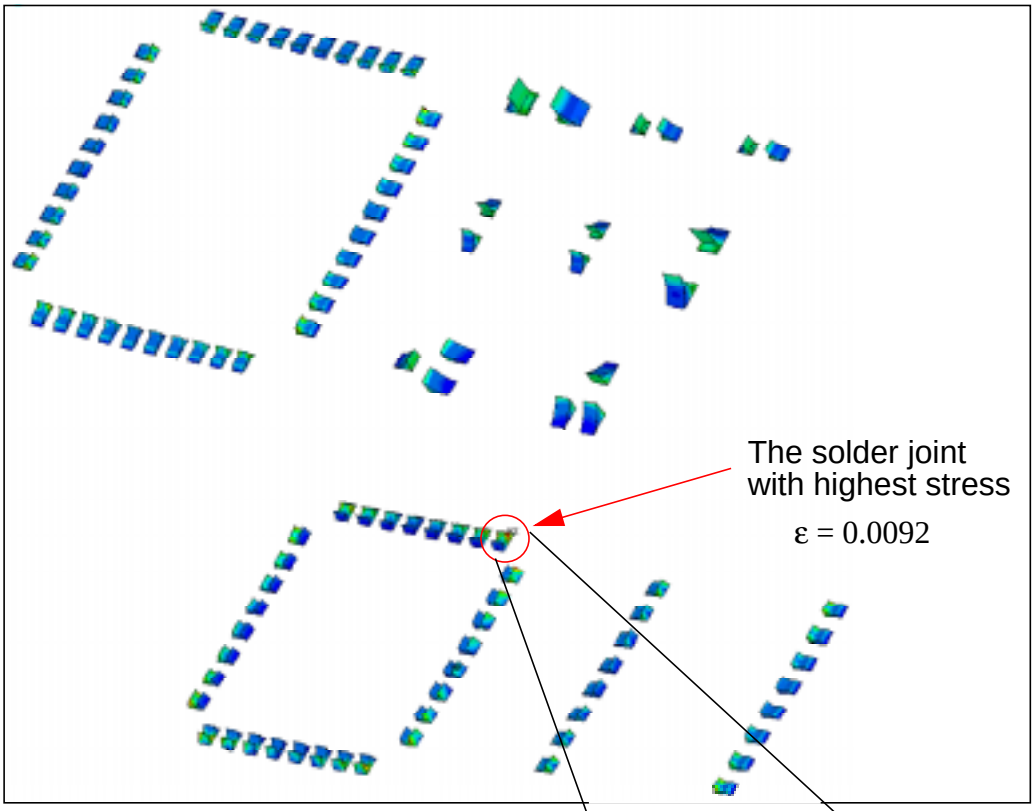
It is important to note that the solution result of a symmetric component is not symmetric. The lower corner DCA and the squared TSOP show non-symmetric stress patterns, due to the existence of neighboring components. Further more, solder joints of a symmetric TSOP component show a non-symmetric result. The stress value of different solder joints, in the same component, are varied by more than 50%. These results can not be obtained by using an isolated component model, or a reduced 2D analysis. These

observations suggest that, in order to identify a “trouble spot”, the 3D board-level modeling and analysis has to be performed.

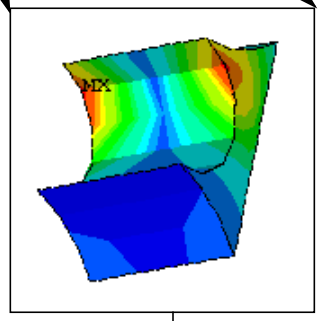
Once the trouble joint is found, more detailed analysis is needed to answer more questions, such as “how bad is this joint?”. This type of analysis is then performed by more detailed local analysis, which is presented in next section.

Table 10.2 Material list in material library.

Material Name	Material No.	E(pascal)	Poisson’s Ratio	CTE (E-6)
PWB (FR4)	1	14e9 (in-plane) 5e9 (out-of-plane	0.16	22.5 (in-plane) 60.0 (out-of-plane)
	2	16e9 (in-plane) 6e9 (out-of-plane)	0.19	20 (in-plane) 50 (out-of-plane)
Solder	1(60pb/40sn)	13e9	0.35	22.5
	2(10pb/90sn)	16e9	0.32	25
Epoxy	1	10e9	0.2	26
	2	7e9	0.3	22
Silicon	1(95%)	176e9	0.33	2.7
	2(80%)	166e9	0.33	3.6
Ceramic	1(AL2O3)	310e9	0.3	6
	2(SiC)	270e9	0.3	3.3
Plastic	1	45e9	0.3	13
	2	48e9	.31	10
Leadframe	1(Copper)	130e9	0.3	17
	2(Alloy)	105e9	0.32	14



1. Global Analysis (Linear - FEA) (a)
   Indicate the worst joint.



ε= 0.015

2. Local Analysis (Nonlinear - FEA) (b)
   Perform more detailed analysis.

3. Local Analysis (Formula) (c)
   Predict life cycle calculation.

$$\overline{N_f} = \frac{1}{2}\left(\frac{\Delta\varepsilon^P}{2\varepsilon_f}\right)^{1/c} = 1407 \text{ (cycle)}$$

Figure 10.11 Global and local analysis for thermomechanical analysis.

10.4.3 Thermal Analysis - Local

Based on the joint indicated in global analysis, a non-linear FE analysis is performed to exam extended thermomechanical behavior. The obtained non-linear results are used to perform a formula based analysis, which is to predict the life cycles of the joint.

As all J-lead solder joints is generated from a master model, that is, all the J-lead solder joints have the same geometry and mesh pattern. The only difference of the bad joint than others are the nodal values of the joint.

In order to perform more detailed analysis on the joint, only the stress and displacement value, associated with this joint, are needed. These stress value are picked by first selecting the nodes of the joint, followed by sorting the node numbers. These displacement and stress results are used as boundary conditions and loads to perform a FE non-linear analysis. The non-linear material property of solder joint is modeled as bi-linear. It is assumed that the stress remains constant. Though the true stress on the solder joint may decrease when the non-linear material properties applied, the change of stress is not considered in this local analysis. This is because the obtained non-linear results will represent the upper bond condition, or the worst case. The non-linear strain obtained in this local is 1.5%, compared to 0.92% in the global analysis.

The formula used for life-cycle prediction is modified Coffin-Manson relation for low cycle fatigue.

$$\overline{N_f} = \frac{1}{2}\left(\frac{\Delta\varepsilon^P}{2\varepsilon_f}\right)^{1/c}$$

where N_f is average cycle to failure, $\Delta\varepsilon^P$ is plastic cyclic strain range, ε_f is fatigue ductility coefficient, and c is fatigue ductility exponent. The constant c is function of temperature T and load frequency f.

$$c = -0.442 - 0.0006T + 0.0174\ln(1 + f)$$

It is assumed that T=40 and f=10 in this case study. The constant c can be obtained by substituting T and f into above equation. The constant ε_f, for 60sn/40pb solder, is about 0.325. Thus, the total life cycle can be calculated as

$$\overline{N_f} = \frac{1}{2}\left(\frac{\Delta\varepsilon^P}{2\varepsilon_f}\right)^{1/c} = \frac{1}{2}\left(\frac{0.015}{0.325}\right)^{-0.424} = 1407$$

10.4.4 Mechanical bending Analysis

Mechanical loadings is one of major factors contributing to product failures. It is generally found in the process of a manufacturing handling and machining depanalization processes. In this bending analysis, the model is clamped on the left-side edge, and force is applied on the right edge. Displacement control is assumed as a mechanical loading. The out-plane displacement applied is as 5% of the total board length. This is a moderate deformed shape encountered in a manufacturing line. The deformed shape of entire board under bending load is shown in Figure 10.12.

10.4.5 Vibrational Analysis

The mechanical behaviors of electrical components under vibrational loads may affect the reliability of the products used in a moving object, such as in automobiles and missiles. The model studied in this case is a populated board clamped on the left side. First 6 natural frequencies and their mode shapes are expanded from the FE calculation. The third mode and its frequency is shown in Figure 10.13.

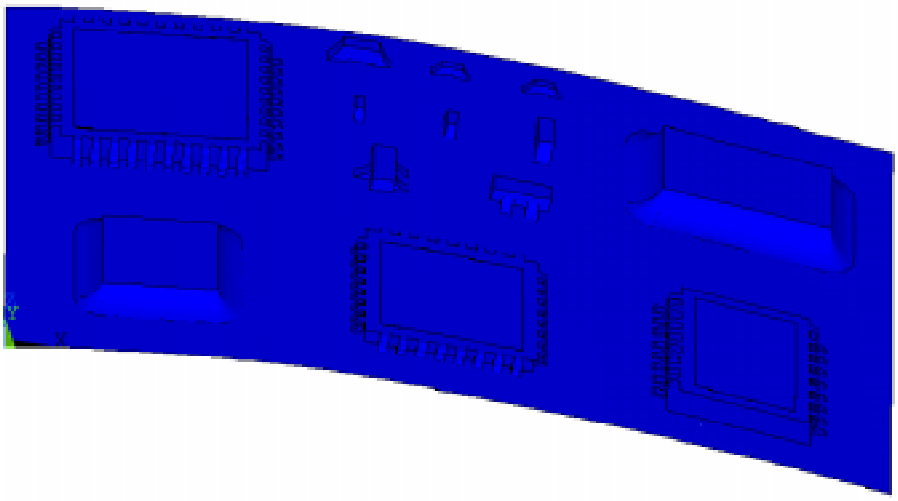


Figure 10.12 Deformed shape of a PWB under mechanical bending load.

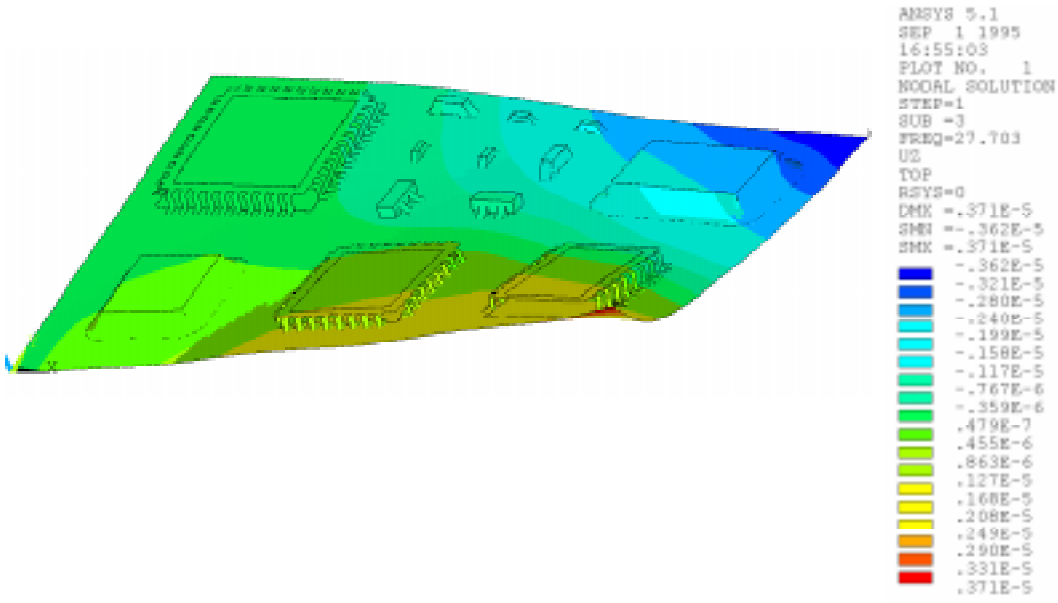


Figure 10.13 Deformed shape of a PWB under vibrational load (mode 3)

10.5 Effectiveness

The developed MP/FEM can provide highly integrated and concurrent design and

analysis capabilities. Mechanical engineers typically concern about the product's physical geometry and material property. Such information is generally available, if a library of electronic component is linked with a library of mechanical components. As a mechanical model can be built as assembling the component icons, the mechanical design or mechanical modeling of a product may be made concurrently when an electronic design decision is made. In the product design, whenever an electronic component is selected and mounted onto the PWB, a mechanical component is selected, correspondingly, from the mechanical library, and assembled onto the PWB simultaneously. Several operations can be predefined on each component for possible later modifications, such as deletion, movement, or even rotation. Thus, a mechanical analysis can be performed at any stage of the design, providing a rapid assessment of any changes in mechanical behavior as the design changes.

A solid model, created by parametric and form rules, is the starting point for the analysis integration. Parametric modeling allows an easy change to a new model by modifying critical dimensions. It also allows the designer to set constraints, and let the software maintain specified properties automatically, such as parallel, alignment, node coupling, etc. A new component, or even an entire product model can be created from parametric based sub-component and sub-product models existing in the component library. Each developed model may link to a modern optimization theory to provide optimization capabilities. The computer can then modify the current designs to create an improved design. With a pre-defined parametric model, a designer of an electronic assembly can implement a mechanical analysis and optimization up front, by specifying analysis type, changing parameters and constraints. A sensitivity study can be performed to predict the variation of geometries.

In this case study, the FE model of a populated board is rapidly and flexibly generated. Different types of analyses have been performed. Upon the author's knowledge, this is the first 3D mechanical model ever built (in the industry and literature) with

detail component geometry on a populated PWB. Based on the benchmark works conducted at one of the member companies, this modeling methodology may reduce modeling cycle time by 100X. The model building time of a board with 10 to 100 components will take about 10 minutes to 8 hours on IBM RISC MR590a workstation.

Part IV

Conclusions and Future Works

From the study results, it concludes that the developed methodology is a very cost-effective and vital tool for thermomechanical design of an electronic product. The summary and the significance of the research is presented in Chapter 11. The limitations of the methodology discussed in this thesis, and proposed work for future consideration, are listed in Chapter 12.

Chapter 11

Conclusions

To address the increasing need for thermomechanical design in a seamless electronic design environment, the new approach, Modularized & Parametric Finite Element Modeling, has been presented. From the study results, it can be concluded that the developed methodology is a very cost-effective and vital tool for designing an electrical product. The developed MP/FEM approach is summarized in Section 11.1. The significance of this new modeling methodology, and the contribution of this research work are presented in section 11.2.

11.1 Research Summary

Based on the observation that there are limited components used to fabricate a product, and limited types of interconnections in a component assembly, a novel approach, so called Modularized & Parametric Finite Element Modeling methodology, has been developed to provide a promising capability for analyzing an entire featured electronic product in much less time without loss of accuracy. Because most products are not designed from scratch, but are instead chosen from an electronic component library, the taxonomic technique is applied to classify the components into a limited number of categories, such as a chip, a resistor or capacitor. Similar to components, most of the substrate, or the interconnection, can be also limited to Plate Through Hole

(PTH), Surface Mount Technology (SMT), Wirebonding (WB), Taped Automatic Bonding (TAB), or Flip Chip, Ball Grid Array(BGA).

In mechanical design analysis, these electronic products are treated as an assembly of typical components, which have been classified and saved into a mechanical component library. Each component is created as a combination of predefined MGP modules. MGP modules are the most basic building blocks to form a electronic product. Each mechanical model of a component is an analysis-ready FE module. This module is different from a meshed FE model, as its geometry, mesh shape, and density are created by built-in parameters and form rules. Each module has a different type of analysis capability, such as static-structural, static-heat transfer, transient heat transfer, or modal analysis. Each module can be further encapsulated into a higher level module.

The parts list generated, by an electrical design, is assumed to be in the form of a link-list. This link-list provides enough information for current mechanical modeling capability. The information is used to link an electronic component library to a mechanical component library. Whenever an electronic component is selected and mounted onto PWB, a corresponding mechanical component is selected from the mechanical library and assembled to PWB simultaneously.

The PWB (substrate) is be broken down to small pieces, according to the location of components mounted on the board and the configuration of board geometry. These small pieces are individually reduced to an equivalent element, which has similar stiffness(property) and behavior. They are then assembled back to represent the original board.

Multilevel (zoom-in) analysis is utilized in the solution procedure. Global prediction (FEA), local analysis (FEA), and detail calculation (formula) are performed step by step until a desired solution is obtained. In zoom-in step, geometry and analysis type are easily modified.

In addition to the regular finite element analysis, the following techniques have

been merged into MP/FEM to achieve highly integrated E/MCAD system: taxonomic technique; feature-based parametric language; global/local analysis - Zoom in/out analysis capability; divide-and-conquer algorithm; graph theory; object oriented concept; and database. Each of the computational techniques and controlling algorithms presented above have been investigated. A computer code, which utilizes these algorithms, has been developed to interface with the "ANSYS" software package.

Two case studies have been performed and tested in a member company of MaRC. The first case, parametric FEA for FCOB reliability, is parametrically performed. The analysis, based on different parameters, is a systematic study for better understanding the thermomechanical behavior of a FCOB. The results of the sensitivity studies can be used to generate design rules of FCOB. In the second case, a FE model is developed for a populated board. The FE model is a board-level mechanical model with detail solder joint connections. Global and local analysis is applied in solution pass. Thermal, mechanical bending, and vibrational analyses have been performed. The worst solder joint under thermal load is identified by a coarse global FE analysis. A more detailed FE analysis is continued to exam the joint connection. The cycle life of the joint is predict by using a formula based tool.

11.2 Significance and contributions

Several computational techniques and controlling algorithms have been integrated into standard FEA to provide fast and concurrent thermomechanical analysis capability.

To reduce the modeling repetition, concepts of taxonomy and thermomechanical component library have been introduced. A thermomechanical component can be generated as a shared, manageable FE model. It can be handled as an icon (modularized FE model) for computational simulation of the movement/replacement of an electronic

component.

Since a geometric sensitivity and uncertainty study is one of the key parts in thermomechanical design and optimization, flexible modeling capability is greatly needed. Pure traditional geometry parameter modeling and/or FEM no longer satisfy this needs. To improve the deficiency, parametric finite element modeling presented in this thesis includes both geometry parameter creation and mesh parameter control in the modeling process. In addition, relations, such as "with/without" and "if-then" relations, are extensively treated as parameters in creating a model. A single model can be used for different tasks, materials, configurations, and conditions. Significant time savings have been found as the result of this one-to-many modeling.

Utilization of concepts of modularization and feature based parameters provide a capability of coupling thermomechanical design with electronic design. While a new electronic component is added to existing design, a corresponding mechanical module can be assembled to the model, and ready for a solution. "What-if" scenarios can be performed with design changes. Failure modes can be recognized and eliminated before final product design, and thus generate a "failure-free" product, which is "correct by design". This single pass design will result in time and cost savings.

While determining the thermomechanical characteristics of a populated board is important, no such analysis has ever been performed. The complexity of geometry and lack of modeling methodology are major obstacles. PWB is generally modeled as a uniform layer with a material property from an experimental test of a piece of specimen, however, its material properties vary significantly from site to site due to nonuniform distribution of copper. "Divide-and-Conquer" and Match-of-inertia methods can be applied for a more detailed PWB modeling. It has been demonstrated that MP/FEM can be applied to model a populated board in a simple manner.

The mechanical complexity of advanced electronic systems and the throughput limitations of existing computing platforms preclude the use of numerical models for

detailed design. The thesis has developed a modeling methodology upon finite element solution within a few integrated controlling algorithms. As a result, the innovative concepts addressed in this thesis should be of particular value to design engineers, concerned with product reliability, performance, cost, and “time-to-market”.

Chapter 12

Limitations and Future Work

As a closing remark of this research work, the limitations of the methodology discussed in this thesis, and proposed work for future consideration, are listed as follows:

1. Need more surface-mount components. In order to create a complete component library for mechanical design of electrical products, more SMT components and peripheral parts have to be studied.

2. Need models for plate-through-hole (PTH) components. Since lots of electrical products use hybrid technology, which includes both SMT and PTH components, in product design, a PTH component library has to be generated, with the SMT component library, to offer more practical utilization of MP/FEM approach.

3. Need better user interface. The MP/FEM methodology is currently implemented by series input files. These files have to be customized to simulate a mechanical design and analysis process. It is desired that the mechanical component models be "picked and placed" through a window-based environment. Some of this feature is currently being developed.

4. Need a data structure for integration of ECAD and MCAD. Currently, the geometric data and format of electrical components, used for mechanical design and analysis, can not be automatically filtered by mechanical design software. The data mapping and translation between an ECAD system and a MCAD system have to be standardized. This is an important aspect in developing an integrated design system.

5. Need a check for conflict of components placement. In this thesis work, the conflict of components can not be checked. The conflict implies that two components are, mistakenly, overlapped. This conflict may result in an interrupt in an analysis calculation. Free of conflict is enforced by manual check in this thesis development.

6. Need more analysis types. As different electrical products may work under different harsh and complex environments, more analysis types are needed to simulate the real situation, such as thermal convection and shock impact.

7. Need better options of p- and h- element type for mesh refinement. The element refinement is implemented by reducing element size and adding mid-side nodes. More refinement options, such as adding more h- and p- version elements, may be developed to perform automatic and dynamical mesh control and modification.

8. Need vias in current model. The vias on the board have been ignored. No via model has been developed in this thesis. Based on the taxonomic technique, three types of via models have to be developed. These three via models are adequate to perform the analysis of a populated board with vias.

9.Need for two side PWB. The developed MP/FEM can be only used for a single side board at current stage. The capability of modeling two side board is currently under investigation.

10. Need generic software platform for modeling. The developed program code can only be implemented under ANSYS software environment. A neutral code, that can be linked with general mechanical design software, is considered as a part of future work.

Apendix A

List of Program

The code used in the thesis are list in this Appendix. The program consists three main parts: 1) MAIN input program, 2) MACRO(subroutine) program, and 3) data file. The programs and comments are listed as follows:

Part 1. MAIN input program:

```
/prep7          ! start pre-processor.
et,2,45         ! two element types are used: Solid-45 and Shell-63.
et,1,63
pre_def         ! predefinitions that are specified in PRE_DEF macro.
csys,11
WPAVE       ! Specify local coodinate system.
*MSG,WARN
ASSEMBLE FCOB-01
*ULIB,compont,lib             ! the program format for creating a component.
*USE,C_FCOB,'FCOB1'    ! The *UIB specify  component file, which is component.lib
                        ! The *USE specify the component to be used, and the
                            !  geometry data file associated with this component.
                            ! C_FCOB is the component type, and the FCOB1 is the
                            geometry data block.
*ULIB,compont,lib
*USE,TSOP_I,'I_lead1','BLOCK1','SOLD_I1','PWB_I1'
! Similar to C_FOB, A TSOP_I is the component type and I_lead1, BLOCK1, and SOLD_I1 are
its MGPs.
*ULIB,compont,lib
! TSOP_J means a component with J-leads on its sode.
*USE,TSOP_J,'J_lead2','BLOCK2','SOLD_J2','PWB_J2'
*ULIB,compont,lib
! C_RE3 applys to a passive component with three solder joints.
*USE,C_RE3,'RE3_1'
```

```
*ULIB,compont,lib
*USE,C_RE3,'RE3_2'
*ULIB,compont,lib
! C_RE2 applys to a passive component with 2 solder joints.
*USE,C_RE2,'RE2_1'
*ULIB,compont,lib
*USE,C_RE2,'RE2_2'
*ULIB,compont,lib
*USE,C_RE2,'RE2_3'
*ULIB,compont,lib
*USE,C_RE2,'RE2_4'
*ULIB,compont,lib
*USE,C_RE2,'RE2_5'
*ULIB,compont,lib
*USE,C_RE2,'RE2_6'
*ULIB,compont,lib
*USE,TSOP_I,'I_lead3','BLOCK3','SOLD_I3','PWB_I3'
*ULIB,compont,lib
*USE,C_FCOB,'FCOB2'
!KSEL,S,LOC,X,-300,400
! the following 8 lines are used as book keeping  commands.
!KDEL,ALL
ALLS
CSYS,0
WPAVE
alls
aslv
aclear,all
alls

!DEFINE ELEMENTS COLOR.
/plopt,defa
/plott,info,off
ESEL,S,MAT,,SILICON
/COLOR,elem,BMAG
ESEL,S,MAT,,EPOXY
/COLOR,ELEM,ORAN
ESEL,S,MAT,,PLAS1
/COLOR,ELEM,GREEN
ESEL,S,MAT,,SOLDER
/COLOR,ELEM,RED
ESEL,S,MAT,,LEAD1
/COLOR,ELEM,BLUE
! Merge all the coincident items, include key points, element, and constraints.
ALLS
KSLL
KSEL,INVE
```

```
KDEL,ALL
ALLS
NUMMRG,NODE,2e-4
NUMMRG,KP
NUMMRG,ELEM
NUMMRG,CE
! Desired analysis type starts after this line.
```

Part 2. Component Library Input File:
C* PARTS2.LIB**

```
RE3
C*** Generate a resistor with 2 and 3 solder joints.
C*** RE3 Create KP= 87, LINE=173, AREA=115, VOLU=23
NUM_OFF,90,175,115,25
*ULIB,data,lib
*USE,arg1
WV1=2*(MY+W)+SY
WV2=(WV1-W)/2/2
k,1,0,,H1
k,2,L1,,H1
k,3,2*L1,,H1
k,4,0,WV2,h1
k,5,L1,WV1/5,h1
k,6,2*L1,MY,h1
k,7,0,2*WV2,h1
k,8,L1,WV1/5*2,h1
k,9,2*L1,MY+W,h1
k,10,0,2*WV2+W,h1
k,11,L1,WV1/5*3,h1
k,12,2*L1,MY+W+SY,h1
k,13,0,WV1-WV2,h1
k,14,L1,WV1/5*4,h1
k,15,2*L1,MY+W+SY+W,h1
k,16,0,WV1,h1
k,17,L1,WV1,h1
k,18,2*L1,WV1,h1
l,1,4
*repeat,5,3,3
l,3,6
*repeat,5,3,3
k,19,2*L1,MY
k,20,2*L1+L2,MY
k,21,2*L1,MY,H1+H2
k,22,2*L1+L2,MY,H1+H2
larc,21,20,22,R
```

```
k,23,2*L1,MY+W+SY
k,24,2*L1+L2,MY+W+SY
k,25,2*L1,MY+W+SY,H1+H2
k,26,2*L1+L2,MY+W+SY,H1+H2
larc,25,24,26,R
k,27,,WV2*2
k,28,-L2,WV2*2
k,29,,WV2*2,H1+H2
k,30,-L2,WV2*2,H1+H2
larc,28,29,30,R
a,6,19,20,21
a,12,23,24,25
a,7,29,28,27
!Define line division for solder profile areas.
 lsel,s,line,,14
 lsel,a,line,,17
 lsel,a,line,,22
 lesize,all,,,DH1
 lsel,s,line,,15
 lsel,a,line,,18
 lsel,a,line,,21
 lesize,all,,,DL2
 lsel,s,line,,16
 lsel,a,line,,19
 lsel,a,line,,20
 lesize,all,,,DH2
 alls
 lccat,14,16
 lccat,17,19
 lccat,20,22
 TYPE,1
 MAT,M_NO1
 R,R_NO1,RV1
 ESHAPE,2
 AMESH,1,3
 a,1,2,5,4
 *repeat,5,3,3,3,3
 a,2,3,6,5
 *repeat,5,3,3,3,3
 !start line div. on Areas.
 lsel,s,loc,x,L1*0.1,L1*0.9
 lsel,a,loc,x,L1*1.1,L1*1.9
 lesize,all,,,DL1
 lsel,s,line,,1
 lsel,a,line,,5
 lsel,a,line,,6
 lsel,a,line,,10
```

```
 lesize,all,,,DMY
 lsel,s,line,,2,4
 lsel,a,line,,7,9
 lesize,all,,,DW
 alls
 AMESH,4,13
!Start ext to Re block.
 LDEL,23,25
 MAT,M_NO2  ! for solder fillet.
 TYPE,2
 ESIZE,,DW
 VEXT,1,3,,,W
 MAT,M_NO3  ! for Re block.
 TYPE,2
 ESIZE,,DH2
 VEXT,4,13,,,,H2
 ASEL,S,LOC,Z,H1+H2
 TYPE,1
 MAT,M_NO1 $R,R_NO1,R_V1
 AMESH,ALL
 TYPE,2 $MAT,M_NO3
 ESIZE,,DH3
 VEXT,ALL,,,,,H3
k,79  ! NO USE SCRATCH POINT.
k,80,-L2,MY
k,81,,MY
k,82,-L2,MY+2*W+SY
k,83,,MY+2*W+SY
k,84,-(L2+LL),MY-LH
k,85,2*L1+L2+LR,MY-LH
k,86,2*L1+L2+LR,MY+2*W+SY+UH
k,87,-(L2+LL),MY+2*W+SY+UH
a,80,81,27,28
a,81,19,33,27
a,27,33,23,39
a,33,34,24,23
a,42,39,83,82
a,39,23,37,83
a,84,85,20,19,81,80
a,85,86,38,24,34,20
a,82,83,37,38,86,87
a,84,80,28,42,82,87
a,19,20,34,33
a,23,24,38,37
a,28,27,39,42
! Line div. for PWB.
 lsel,s,line,,166
```

```
 lesize,all,,,DLH
 lsel,s,line,,169
 lesize,all,,,DLR
 lsel,s,line,,171
 lesize,all,,,DUH
 lsel,s,line,,173
 lesize,all,,,DLL
 lsel,s,line,,168
 lesize,all,,,D_1
 lsel,s,line,,167
 lesize,all,,,D_2
 lsel,s,line,,170
 lesize,all,,,D_3
 lsel,s,line,,172
 lesize,all,,,D_4
 lsel,s,line,,157,158
 lsel,a,line,,160,165,5
 lesize,all,,,DL11
 MAT,M_NO4 $TYPE,1 $R,R_NO4,R_V4
 AMESH,104,105
 AMESH,108
 AMESH,103
 AMESH,106
 AMESH,107
 AMESH,113,115
 ESHAPE, $ AMESH,109,112
 ALLS
/eof


RE2
C*** Generate a RESISTOR with 2-solder JOINTS on Side
C*** Create kp=63, line=96, area=49, volu=7
NUM_OFF,63,96,49,7
*ULIB,data,lib
*USE,arg1
!Generate halp of the Solder fillet, then copy.
k,1
k,2,L1
k,3,L1+L2
K,4,,H1
k,5,L1,H1
K,6,,H1+H2
K,7,L1,H1+H2
k,8,L1+L2,H1+H2
larc,7,3,8,R
a,1,2,5,4
```

```
a,2,3,7,5
a,4,5,7,6
!Start line div. control.
lsel,s,loc,x,L1*0.1,L1*0.9
LESIZE,ALL,,,DL1
LSEL,S,LINE,,7,9,2
LESIZE,ALL,,,DH2
LSEL,S,LINE,,3,5,2
LESIZE,ALL,,,DH1
ALLS
LCCAT,3,7
MAT,M_NO1
TYPE,1 $ESHAPE,2
R,R_NO1,R_V1
AMESH,1,3,2
AMESH,2
LDEL,10
ESIZE,,DW
TYPE,2
MAT,M_NO2
VEXT,1,2,,,,-W
MAT,M_NO3
VEXT,3,,,,,-W
!Generate Center Block.
BLOCK,-L3,0,H1,H1+H2,-W,0
LSEL,S,LINE,,39,42
LESIZE,ALL,,,DW
LSEL,S,LINE,,31,33,2
LSEL,A,LINE,,36,38,2
LESIZE,ALL,,,DH2
LSEL,S,LINE,,32,34,2
LSEL,A,LINE,,35,37,2
LESIZE,ALL,,,DL3,-3
TYPE,2
MAT,M_NO3
VMESH,4
ALLS
!COPY to another side.
LOCAL,15,0,XYZ11-L3,XYZ11,XYZ11-W,,,180
CSYS,11
!VTRAN,15,1,3,,,,1
VTRAN,15,1,3
LOCAL,15,0,XYZ11+W+LL,XYZ11+L3+L2+L1+LH,XYZ11,90,90
CSYS,11
VTRAN,15,1,7,,,,1
!Create AREA of PWB
 CSYS,11
```

```
k,48,
k,49,LL+W+LR
k,50,LL+W+LR,LH+2*(L1+L2)+L3+UH
k,51,0,LH+2*(L1+L2)+L3+UH
k,52,LL,LH
k,53,LL,LH+L2
k,54,LL,LH+L1+L2
k,55,LL,LH+L1+L2+L3
k,56,LL,LH+L1+L2+L3+L1
k,57,LL,LH+L1+L2+L3+L1+L2
k,58,LL+W,LH
k,59,LL+W,LH+L2
k,60,LL+W,LH+L1+L2
k,61,LL+W,LH+L1+L2+L3
k,62,LL+W,LH+L1+L2+L3+L1
k,63,LL+W,LH+L1+L2+L3+L1+L2
a,48,52,53,54,55,56,57,51
a,48,49,58,52
a,58,49,50,63,62,61,60,59
a,63,50,51,57
a,52,58,59,53
*REPEAT,5,1,1,1,1
LESIZE,73,,,D1
LESIZE,82,,,D2
LESIZE,85,,,D3
LESIZE,79,,,D4
LESIZE,80,,,DLL
LESIZE,81,,,DLH
LESIZE,84,,,DLR
LESIZE,91,,,DUH
LSEL,S,LINE,,74,90,16
LSEL,A,LINE,,78,86,8
LESIZE,ALL,,,DL2
LSEL,S,LINE,,75,89,14
LSEL,A,LINE,,77,87,10
LESIZE,ALL,,,DL1
LSEL,S,LINE,,76,88,12
LESIZE,ALL,,,DL3*0.9
LSEL,S,LOC,X,LL*1.005,LL+W*0.99
LSEL,R,LOC,Y,LH*0.99,LH+2*(L1+L2)+L3-L2*0.001
LSEL,R,LOC,Z,0
LESIZE,ALL,,,DW
ALLS
MAT,M_NO4
TYPE,1
R,R_NO4,R_V4
ESHAPE,2
```

```
 AMESH,45,49
 ESHAPE,
 AMESH,41,44
/eof

I_LEAD
C*** This is 3D Shell Model for a I-Lead
*ULIB,data,lib
*USE,arg1
NUM_OFF,16,18,5,0
k,1,,R2+H+R1
k,2,L1,R2+H+R1
k,3,L1+R1,R2+H
k,4,L1+R1,R2
k,5,L1+R1+R2
k,6,L1+R1+R2+L2
k,7,L1,R2+H
k,8,L1+R1+R2,R2
k,9,,R2+H+R1,-W
l,1,2
LARC,3,2,7,R1
l,3,4
LARC,4,5,8,R2
l,5,6
l,1,9
ADRAG,1,2,3,4,5,,6
LESIZE,1,,,DL1
LESIZE,2,,,DR1
LESIZE,3,,,DH
LESIZE,4,,,DR2
LESIZE,5,,,DL2
LSEL,S,LOC,Z,-W*0.9,-W*0.1
LESIZE,ALL,,,DW
MAT,M_NO1
TYPE,1
R,R_NO1,R_V1
REAL,R_NO1
ESHAPE,2
AMESH,1,5
LDEL,6
ALLS
/EOF


BLOCK
C*** Define a Block
```

```
C*** This Lib. Fun Generate Volu=0
C***                AREA=4*(NX+NY)+NXC*NYC
C***                LINE=4*AREA
C***                KP=4*AREA
*ULIB,data,lib
*USE,arg1
WV1=4*(NX+NY)+NXC*NYC
NUM_OFF,4*WV1,4*WV1,WV1,0
! Lower Side area creation.
RECT,0,MX,0,MY
WPOFF,MX
*DO,I,1,NX-1,1
 RECT,0,W,0,MY
 WPOFF,W
 RECT,0,SX,0,MY
 WPOFF,SX
*ENDDO
RECT,0,W,0,MY
WPAVE
WPOFF,,MY
*DO,I,1,NY-1,1
 RECT,0,MX,0,W
 WPOFF,,W
 RECT,0,MX,0,SY
 WPOFF,,SY
*ENDDO
 RECT,0,MX,0,W
WPAVE
!Line div for lwoer and left side.
LSEL,S,LOC,Y,MY*0.1,MY*0.9
LESIZE,ALL,,,DMY
LSEL,S,LOC,X,MX*0.1,MX*0.9
LESIZE,ALL,,,DMX
*DO,I,1,NX-1,1
WV1=MX+(I-1)*(W+SX)
LSEL,S,LOC,X,WV1+W*0.01,WV1+W*0.99
LESIZE,ALL,,,DW
LSEL,S,LOC,X,WV1+W+SX*0.01,WV1+W+SX*0.99
LESIZE,ALL,,,DSX
*ENDDO
I=NX
WV1=MX+(I-1)*(W+SX)
LSEL,S,LOC,X,WV1+W*0.01,WV1+W*0.99
LESIZE,ALL,,,DW
*DO,I,1,NY-1,1
WV1=MY+(I-1)*(W+SY)
LSEL,S,LOC,Y,WV1+W*0.01,WV1+W*0.99
```

```
LESIZE,ALL,,,DW
LSEL,S,LOC,Y,WV1+W+SY*0.01,WV1+W+SY*0.99
LESIZE,ALL,,,DSY
*ENDDO
I=NY
WV1=MY+(I-1)*(W+SY)
LSEL,S,LOC,Y,WV1+W*0.01,WV1+W*0.99
LESIZE,ALL,,,DW
ALLS
ASEL,S,LOC,Y,0,MY
LOCAL,15,0,XYZ11,XYZ11+MY+(NY-1)*(W+SY)+W,XYZ11
CSYS,11
ATRAN,15,ALL
ASEL,S,LOC,X,0,MX
LOCAL,15,0,XYZ11+MX+(NX-1)*(W+SX)+W,XYZ11,XYZ11
CSYS,11
ATRAN,15,ALL
WPAVE
WV1=(NX*(W+SX)-SX)/NXC
WV2=(NY*(W+SY)-SY)/NYC
*DO,I,1,NXC,1
*DO,J,1,NYC,1
 WPOFF,MX+(I-1)*WV1,MY+(J-1)*WV2
 RECT,0,WV1,0,WV2
 WPAVE
*ENDDO
*ENDDO
ASEL,S,LOC,X,MX,MX+NX*(W+SX)-SX
ASEL,R,LOC,Y,MY,MY+NY*(W+SY)-SY
LSLA
LESIZE,ALL,,,1
ALLS
TYPE,1
MAT,M_NO1
R,R_NO1,R_V1
REAL,R_NO1
AMESH,1,4*(NX+NY)+NXC*NYC
ALLS
*DO,I,1,NXC,1
 ASEL,S,LOC,X,MX+(I-1)*WV1,MX+I*WV1
 ASEL,R,LOC,Y,MY,MY+WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,MY
 NSEL,R,LOC,X,MX+(I-1)*WV1,MX+I*WV1
 CEINTF
```

```
*ENDDO
ALLS
*DO,I,1,NXC,1
 ASEL,S,LOC,X,MX+(I-1)*WV1,MX+I*WV1
 ASEL,R,LOC,Y,MY+(NYC-1)*WV2,MY+NYC*WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,MY+NYC*WV2
 NSEL,R,LOC,X,MX+(I-1)*WV1,MX+I*WV1
 CEINTF
*ENDDO
ALLS
*DO,I,1,NYC
 ASEL,S,LOC,X,MX,MX+WV1
 ASEL,R,LOC,Y,MY+(I-1)*WV2,MY+I*WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,MX
 NSEL,R,LOC,Y,MY+(I-1)*WV2,MY+I*WV2
 CEINTF
*ENDDO
ALLS
*DO,I,1,NYC
 ASEL,S,LOC,X,MX+(NXC-1)*WV1,MX+NXC*WV1
 ASEL,R,LOC,Y,MY+(I-1)*WV2,MY+I*WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,MX+NXC*WV1
 NSEL,R,LOC,Y,MY+(I-1)*WV2,MY+I*WV2
 CEINTF
*ENDDO
ALLS

/EOF

PWB_I
C*** Create a PWB Patch for a I-lead component.
C*** This Module produce VOLU=0
C***                AREA=4*(NX+NY)+NXC*NYC+16
C***                LINE=4*area
C***                KP=4*area
*ULIB,data,lib
*USE,arg1     !Lead Info.
*USE,arg2     !Block Info.
```

```
*USE,arg3      !solder Info.
*USE,arg4      !Board Info.
WV0=4*(NX+NY)+NXC*NYC+8
NUM_OFF,4*WV0+32,4*WV0+32,WV0+8,0
WV1=2*(MX+L1-L2P+R1+R2)+NX*(W+SX)-SX
WV2=2*(MY+L1-L2P+R1+R2)+NY*(W+SY)-SY
WV3=L2+L2P+L2M
k,1,-LL,-LH
k,2,2*WV3+WV1+LR,-LH
k,3,2*WV3+WV1+LR,2*WV3+WV2+UH
k,4,-LL,2*WV3+WV2+UH
k,5,0,0
k,6,2*WV3+WV1,0
k,8,0,2*WV3+WV2
k,7,2*WV3+WV1,2*WV3+WV2
!Areas on lower side.
RECT,0,WV3,0,WV3
WPOFF,WV3
RECT,0,MX+L1-L2P+R1+R2,0,WV3
WPOFF,MX+L1-L2P+R1+R2
*DO,I,1,NX-1,1
 RECT,0,W,0,WV3
 WPOFF,W
 RECT,0,SX,0,WV3
 WPOFF,SX
*ENDDO
I=NX
RECT,0,W,0,WV3
WPOFF,W
RECT,0,MX+L1-L2P+R1+R2,0,WV3
WPAVE
!Areas on left side.
WPOFF,,WV3
RECT,0,WV3,0,MY+L1-L2P+R1+R2
WPOFF,,MY+L1-L2P+R1+R2
*DO,I,1,NY-1,1
 RECT,0,WV3,0,W
 WPOFF,,W
 RECT,0,WV3,0,SY
 WPOFF,,Sy
*ENDDO
I=NY
RECT,0,WV3,0,W
WPOFF,,W
RECT,0,WV3,0,MY+L1-L2P+R1+R2
WPAVE
!Line Div. Control.
```

```
LSEL,S,LOC,Y,WV3*0.05,WV3*0.95
LSEL,A,LOC,X,WV3*0.05,WV3*0.95
LESIZE,ALL,,,DL2+DR2,D_RATIO
LSEL,S,LOC,X,WV3*1.05,WV3+(L1+MX-L2P+R1+R2)*0.95
LESIZE,ALL,,,DMX
LSEL,S,LOC,Y,WV3*1.05,WV3+(L1+MY-L2P+R1+R2)*0.95
LESIZE,ALL,,,DMY
*DO,I,1,NX-1,1
 WV4=WV3+MX+L1-L2P+R1+R2+(I-1)*(SX+W)
 LSEL,S,LOC,X,WV4+W*0.05,WV4+W*0.95
 LESIZE,ALL,,,DW
 LSEL,S,LOC,X,WV4+W+SX*0.05,WV4+W+SX*0.95
 LESIZE,ALL,,,DSX
*ENDDO
I=NX
WV4=WV3+MX+L1-L2P+R1+R2+(I-1)*(SX+W)
LSEL,S,LOC,X,WV4+W*0.05,WV4+W*0.95
LESIZE,ALL,,,DW
LSEL,S,LOC,X,WV4+W+(MX+L1-L2P+R1+R2)*0.05,WV4+W+(MX+L1-L2P+R1+R2)*0.95
LESIZE,ALL,,,DMX
*DO,I,1,NY-1,1
 WV4=WV3+MY+L1-L2P+R1+R2+(I-1)*(SY+W)
 LSEL,S,LOC,Y,WV4+W*0.05,WV4+W*0.95
 LESIZE,ALL,,,DW
 LSEL,S,LOC,Y,WV4+W+SY*0.05,WV4+W+SY*0.95
 LESIZE,ALL,,,DSY
*ENDDO
I=NY
WV4=WV3+MY+L1-L2P+R1+R2+(I-1)*(SY+W)
LSEL,S,LOC,Y,WV4+W*0.05,WV4+W*0.95
LESIZE,ALL,,,DW
LSEL,S,LOC,Y,WV4+W+(MY+L1-L2P+R1+R2)*0.05,WV4+W+(MY+L1-L2P+R1+R2)*0.95
LESIZE,ALL,,,DMY
ALLS
!Copy to right and upper side.
ASEL,S,LOC,Y,0,WV3
LOCAL,15,0,XYZ11,XYZ11+WV3+WV2,XYZ11
CSYS,11
ATRAN,15,ALL
ASEL,S,LOC,X,0,WV3
LOCAL,15,0,XYZ11+WV3+WV1,XYZ11,XYZ11
CSYS,11
ATRAN,15,ALL
WPAVE
WV4=WV1/NXC
WV5=WV2/NYC
*DO,I,1,NXC,1
```

```
*DO,J,1,NYC,1
 WPOFF,WV3+(I-1)*WV4,WV3+(J-1)*WV5
 RECT,0,WV4,0,WV5
 WPAVE
*ENDDO
*ENDDO
ASEL,S,LOC,X,WV3,WV3+WV1
ASEL,R,LOC,Y,WV3,WV3+WV2
LSLA
LESIZE,ALL,,,1
a,1,2,6,5
a,2,3,7,6
a,3,4,8,7
a,1,5,8,4
!Generate additional 8 kp, 12 line, 4 area
ASEL,S,LOC,X,-LL,WV3
ASEL,A,LOC,X,WV3+WV1,WV3+WV1+WV3+LR
ASEL,A,LOC,Y,-LH,WV3
ASEL,A,LOC,Y,WV3+WV2,WV3+WV2+WV3+UH
LSLA
LSEL,R,LOC,X,-LL-1,WV3+WV1+WV3+LR+1   ! ANSYS BUG!!!!
ASLL
KSEL,S,KP,,1,4*WV0+8
NUMMRG,KP
AGLUE,ALL
!Create additional 4 areas.
!Line div. for outer lines
LSEL,S,LOC,Y,-LH
LESIZE,ALL,,,DLH
LSEL,S,LOC,Y,WV3+WV2+WV3+UH
LESIZE,ALL,,,DUH
LSEL,S,LOC,X,-LL
LESIZE,ALL,,,DLL
LSEL,S,LOC,X,WV3+WV1+WV3+LR
LESIZE,ALL,,,DLR
LSEL,S,LOC,X,-LL,0
LSEL,R,LOC,Y,-LH,0
LESIZE,ALL,,,D1
LSEL,S,LOC,X,-LL,0
LSEL,R,LOC,Y,WV3+WV2+WV3,WV3+WV2+WV3+UH
LESIZE,ALL,,,D4
LSEL,S,LOC,X,WV3+WV1+WV3,WV3+WV1+WV3+LR
LSEL,R,LOC,Y,-LH,0
LESIZE,ALL,,,D2
LSEL,S,LOC,X,WV3+WV1+WV3,WV3+WV1+WV3+LR
LSEL,R,LOC,Y,WV3+WV2+WV3,WV3+WV2+WV3+UH
LESIZE,ALL,,,D3
```

```
ALLS
MAT,M_NO1
TYPE,1
R,R_NO1,R_V1
REAL,R_NO1
ESHAPE,2  $AMESH,1,WV0
ESHAPE,  $AMESH,WV0+5,WV0+8

*DO,I,1,NXC,1
 ASEL,S,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 ASEL,R,LOC,Y,WV3,WV3+WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,WV3*0.999,WV3*1.001
 NSEL,R,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 CEINTF
*ENDDO
*DO,I,1,NXC,1
 ASEL,S,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 ASEL,R,LOC,Y,WV3+WV2-WV5,WV3+WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,WV3*0.9999+WV2,WV3*1.0001+WV2
 NSEL,R,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 CEINTF
*ENDDO
*DO,I,1,NYC,1
 ASEL,S,LOC,X,WV3,WV3+WV4
 ASEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,WV3*0.999,WV3*1.001
 NSEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 CEINTF
*ENDDO
*DO,I,1,NYC,1
 ASEL,S,LOC,X,WV3+WV1-WV4,WV3+WV1
 ASEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,WV1+WV3*0.999,WV1+WV3*1.001
 NSEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 CEINTF
```

```
*ENDDO
ALLS
/EOF


SOLD_I
C*** Create a solder joint for a I-lead.
C*** This module generate KP=13, Line=15, AREA=7, VOLU=1
C*** arg1 is lead geo. info.<-I_lead0, arg2 is Solder Geo. info.
*ULIB,data,lib
*USE,arg1
*USE,arg2
NUM_OFF,13,15,7,1
k,1,
k,2,L2P+L2+L2M
k,3,L2P+L2,S_H
k,4,L2P,S_H
k,5,L2P-R2,S_H+R2
k,6,L2P,S_H+R2
k,7,L2P+L2+L2M,S_H
k,8,0,S_H+R2
LARC,5,4,6,R2
LARC,3,2,7,(S_H+L2M)*1.1
LARC,1,5,8,(S_H+L2M+R2)*1.1
A,1,2,3,4,5
LESIZE,1,,,DR2
LESIZE,2,,,DS_H
LESIZE,3,,,DS_H
LESIZE,4,,,DR2+DL2,D_RATIO
LESIZE,5,,,DL2
LCCAT,1,5
TYPE,1
MAT,M_NO1
R,R_NO1,R_V1
REAL,R_NO1
ESHAPE,2
AMESH,1
LDEL,6
TYPE,2
MAT,M_NO2
ESIZE,,DW
VEXT,1,,,,,-W
/EOF

J_LEAD
C*** Create a J_lead Model.
C*** Create KP=15, LINE=17, AREA=5, VOLU=0
```

```
C*** arg1 = J_LEAD0
*ULIB,data,lib
*USE,arg1
NUM_OFF,15,17,5,0
K,1,0,R2+H+R1
K,2,L1,R2+H+R1
K,3,L1+R1,R2+H
K,4,L1+R1,R2
K,5,L1+R1-R2
K,6,L1+R1-2*R2,R2
K,7,L1,R2+H
k,8,L1+R1-R2,R2
K,9,0,R2+H+R1,-W
l,1,2
LARC,3,2,7,R1
L,3,4
LARC,5,4,8,R2
LARC,6,5,8,R2
L,1,9

LESIZE,1,,,DL1
LESIZE,2,,,DR1
LESIZE,3,,,DH
LESIZE,4,,,DR2
LESIZE,5,,,DR2
ADRAG,1,2,3,4,5,,6
LSEL,S,LOC,Z,-W*0.1,-W*0.9
LESIZE,ALL,,,DW
ALLS
TYPE,1
MAT,M_NO1
R,R_NO1,R_V1
REAL,R_NO1
AMESH,1,5
LDEL,6
/EOF

SOLD_J
C*** Define a Solder joint connection for a J-LEAD
C*** Create KP=13, LINE=15, AREA=7, VOLU=1
C*** arg1 = J_LEAD0, arg2 = SOLD_J0
*ULIB,data,lib
*USE,arg1
*USE,arg2
NUM_OFF,13,15,7,1
K,1,
K,2,L2P+2*R2+L2M
```

```
K,3,L2P+2*R2,S_H+R2
K,4,L2P+R2,S_H
K,5,L2P,S_H+R2
K,6,L2P+R2,S_H+R2
K,7,L2P+2*R2+L2M,R2+S_H
K,8,,R2+S_H
LARC,5,4,6,R2
LARC,4,3,6,R2
LARC,3,2,7,(R2+S_H+L2M)*1.1
LARC,1,5,8,(R2+S_H+L2M)*1.1
A,1,2,3,4,5
LESIZE,1,,,DR2
LESIZE,2,,,DR2
LESIZE,3,,,DS_H
LESIZE,4,,,DS_H
LESIZE,5,,,2*DR2,D_RATIO
LCCAT,1,2
ALLS
TYPE,1
MAT,M_NO1
R,R_NO1,R_V1
REAL,R_NO1
ESHAPE,2
AMESH,1
LDEL,6
TYPE,2
MAT,M_NO2
ESIZE,,DW
VEXT,1,,,,,-W
ALLS
/EOF


PWB_J
C*** Create a PWB Patch for a J-lead component.
C*** This Module produce VOLU=0
C***                AREA=4*(NX+NY)+NXC*NYC+16
C***                LINE=4*area
C***                KP=4*area
*ULIB,data,lib
*USE,arg1     !Lead Info.
*USE,arg2     !Block Info.
*USE,arg3     !solder Info.
*USE,arg4     !Board Info.
WV0=4*(NX+NY)+NXC*NYC+8
NUM_OFF,4*WV0+32,4*WV0+32,WV0+8,0
L2=2*R2
```

```
WV1=2*(MX+L1+R1-L2-L2P)+NX*(W+SX)-SX
WV2=2*(MY+L1+R1-L2-L2P)+NY*(W+SY)-SY
WV3=L2M+L2+L2P
k,1,-LL,-LH
k,2,2*WV3+WV1+LR,-LH
k,3,2*WV3+WV1+LR,2*WV3+WV2+UH
k,4,-LL,2*WV3+WV2+UH
k,5,0,0
k,6,2*WV3+WV1,0
k,8,0,2*WV3+WV2
k,7,2*WV3+WV1,2*WV3+WV2
!Areas on lower side.
RECT,0,WV3,0,WV3
WPOFF,WV3
RECT,0,MX+(L1+R1-L2)-L2P,0,WV3
WPOFF,MX+(L1+R1-L2)-L2P
*DO,I,1,NX-1,1
 RECT,0,W,0,WV3
 WPOFF,W
 RECT,0,SX,0,WV3
 WPOFF,SX
*ENDDO
I=NX
RECT,0,W,0,WV3
WPOFF,W
RECT,0,MX+(L1+R1-L2)-L2P,0,WV3
WPAVE

!Areas on left side.
WPOFF,,WV3
RECT,0,WV3,0,MY+(L1+R1-L2)-L2P
WPOFF,,MY+(L1+R1-L2)-L2P
*DO,I,1,NY-1,1
  RECT,0,WV3,0,W
 WPOFF,,W
 RECT,0,WV3,0,SY
 WPOFF,,Sy
*ENDDO
I=NY
RECT,0,WV3,0,W
WPOFF,,W
RECT,0,WV3,0,MY+(L1+R1-L2)-L2P
WPAVE
!Line Div. Control
LSEL,S,LOC,Y,WV3*0.05,WV3*0.95
LSEL,A,LOC,X,WV3*0.05,WV3*0.95
LESIZE,ALL,,,2*DR2,D_RATIO
```

```
!Lower side
LSEL,S,LOC,X,WV3*1.0001,WV3+(MX+(L1+R1-L2)-L2P)*0.995
LESIZE,ALL,,,DMX
*DO,I,1,NX-1,1
 WV4=WV3+MX+L1+R1-L2-L2P+(I-1)*(SX+W)
 LSEL,S,LOC,X,WV4+W*0.05,WV4+W*0.95
 LESIZE,ALL,,,DW
 LSEL,S,LOC,X,WV4+W+SX*0.05,WV4+W+SX*0.95
 LESIZE,ALL,,,DSX
*ENDDO
I=NX
WV4=WV3+MX+L1+R1-L2-L2P+(I-1)*(SX+W)
LSEL,S,LOC,X,WV4+W*0.05,WV4+W*0.95
LESIZE,ALL,,,DW
LSEL,S,LOC,X,WV4+W+(MX+L1+R1-L2-L2P)*0.05,WV4+W+(MX+L1+R1-L2-L2P)*0.95
LESIZE,ALL,,,DMX
LSEL,S,LOC,Y,WV3*1.0001,WV3+(MY+(L1+R1-L2)-L2P)*0.995
LESIZE,ALL,,,DMY
*DO,I,1,NY-1,1
 WV4=WV3+MY+L1+R1-L2-L2P+(I-1)*(SY+W)
 LSEL,S,LOC,Y,WV4+W*0.05,WV4+W*0.95
 LESIZE,ALL,,,DW
 LSEL,S,LOC,Y,WV4+W+SY*0.05,WV4+W+SY*0.95
 LESIZE,ALL,,,DSY
*ENDDO
I=NY
WV4=WV3+MY+L1+R1-L2-L2P+(I-1)*(SY+W)
LSEL,S,LOC,Y,WV4+W*0.05,WV4+W*0.95
LESIZE,ALL,,,DW
LSEL,S,LOC,Y,WV4+W+(MY+L1+R1-L2-L2P)*0.05,WV4+W+(MY+L1+R1-L2-L2P)*0.95
LESIZE,ALL,,,DMY
!Copy lower and left side to upper and right side
ASEL,S,LOC,Y,0,WV3
LOCAL,15,0,XYZ11,XYZ11+WV3+WV2,XYZ11
CSYS,11
ATRAN,15,ALL
ASEL,S,LOC,X,0,WV3
LOCAL,15,0,XYZ11+WV3+WV1,XYZ11,XYZ11
CSYS,11
ATRAN,15,ALL

WPAVE
WV4=WV1/NXC
WV5=WV2/NYC
*DO,I,1,NXC,1
*DO,J,1,NYC,1
 WPOFF,WV3+(I-1)*WV4,WV3+(J-1)*WV5
```

```
 RECT,0,WV4,0,WV5
 WPAVE
*ENDDO
*ENDDO
ASEL,S,LOC,X,WV3,WV3+WV1
ASEL,R,LOC,Y,WV3,WV3+WV2
LSLA
LESIZE,ALL,,,1
a,1,2,6,5
a,2,3,7,6
a,3,4,8,7
a,1,5,8,4
!Generate additional 8 kp, 12 line, 4 area
ASEL,S,LOC,X,-LL,WV3
ASEL,A,LOC,X,WV3+WV1,WV3+WV1+WV3+LR
ASEL,A,LOC,Y,-LH,WV3
ASEL,A,LOC,Y,WV3+WV2,WV3+WV2+WV3+UH
LSLA
LSEL,R,LOC,X,-LL-1,WV3+WV1+WV3+LR+1   !ANSYS BUGS
ASLL
KSLL
NUMMRG,KP
AGLUE,ALL
!Create additional 4 areas.
LSEL,S,LOC,Y,-LH
LESIZE,ALL,,,DLH
LSEL,S,LOC,Y,WV3+WV2+WV3+UH
LESIZE,ALL,,,DUH
LSEL,S,LOC,X,-LL
LESIZE,ALL,,,DLL
LSEL,S,LOC,X,WV3+WV1+WV3+LR
LESIZE,ALL,,,DLR
LSEL,S,LOC,X,-LL,0
LSEL,R,LOC,Y,-LH,0
LESIZE,ALL,,,D1
LSEL,S,LOC,X,-LL,0
LSEL,R,LOC,Y,WV3+WV2+WV3,WV3+WV2+WV3+UH
LESIZE,ALL,,,D4
LSEL,S,LOC,X,WV3+WV1+WV3,WV3+WV1+WV3+LR
LSEL,R,LOC,Y,-LH,0
LESIZE,ALL,,,D2
LSEL,S,LOC,X,WV3+WV1+WV3,WV3+WV1+WV3+LR
LSEL,R,LOC,Y,WV3+WV2+WV3,WV3+WV2+WV3+UH
LESIZE,ALL,,,D3
ALLS
MAT,M_NO1
TYPE,1
```

```
R,R_NO1,R_V1
REAL,R_NO1
ESHAPE,2   $AMESH,1,WV0
ESHAPE,   $AMESH,WV0+5,WV0+8
*DO,I,1,NXC,1
 ASEL,S,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 ASEL,R,LOC,Y,WV3,WV3+WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,WV3*0.999,WV3*1.001
 NSEL,R,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 CEINTF
*ENDDO
*DO,I,1,NXC,1
 ASEL,S,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 ASEL,R,LOC,Y,WV3+WV2-WV5,WV3+WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,WV3*0.9999+WV2,WV3*1.0001+WV2
 NSEL,R,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 CEINTF
*ENDDO
*DO,I,1,NYC,1
 ASEL,S,LOC,X,WV3,WV3+WV4
 ASEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,WV3*0.999,WV3*1.001
 NSEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 CEINTF
*ENDDO
*DO,I,1,NYC,1
 ASEL,S,LOC,X,WV3+WV1-WV4,WV3+WV1
 ASEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,WV1+WV3*0.999,WV1+WV3*1.001
 NSEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 CEINTF
*ENDDO
ALLS
/EOF
```

```
FCOB
C*** Create a Flip-Chip with Board.
C*** Generate KP=80, Line=120, AREA=60, VOLU=12
*ULIB,data,lib
*USE,arg1
NUM_OFF,80,100,60,12
K,1,L1/2,-L2/2
K,2,L1/2+F_L,-L2/2
K,3,L1/2,-L2/2,H1
K,4,L1/2,-L2/2,H1+H2
K,5,L1/2+F_L,-L2/2,H1+H2
LARC,4,2,5,R
A,1,2,4,3
LESIZE,1,,,DR,-2
LESIZE,2,,,DF_L
LESIZE,3,,,DH2
LESIZE,4,,,DH1
MAT,M_NO1
TYPE,1
R,R_NO1,R_V1
REAL,R_NO1
AMESH,1
MAT,M_NO2  $ TYPE,2
ESIZE,,DRO
VROT,1,,,,,,4,1,90
ESIZE,,DL2
VEXT,1,,,,L2
MAT,M_NO1  $TYPE,1  $REAL,R_NO1
AMESH,4
MAT,M_NO2  $TYPE,2
ESIZE,,DL1
VEXT,4,,,-L1
LOCAL,15,0,XYZ11,XYZ11,XYZ11,180
CSYS,11
VTRAN,15,1,3
LOCAL,14,0,XYZ11+L1/2,XYZ11-L2/2,XYZ11
LOCAL,15,0,XYZ11+L1/2,XYZ11+L2/2,XYZ11,90
CSYS,14
VTRAN,15,1
LOCAL,15,0,XYZ11-L1/2,XYZ11-L2/2,XYZ11,270
CSYS,14
VTRAN,15,1
CSYS,11
BLOCK,-L1/2,L1/2,-L2/2,L2/2,0,H1
BLOCK,-L1/2,L1/2,-L2/2,L2/2,H1,H1+H2
VSEL,S,VOLU,,9,10
```

```
ASLV
LSLA
LSEL,R,LOC,Z,0+H1*0.1,H1*0.9
LESIZE,ALL,,,DH1
LSLA
LSEL,R,LOC,Z,H1+H2*0.1,H1+H2*0.9
LESIZE,ALL,,,DH2
LSLA
LSEL,R,LOC,X,-L1/2*0.9,L1/2*0.9
LESIZE,ALL,,,DL1
LSLA
LSEL,R,LOC,Y,-L2/2*0.1,L2/2*0.1
LESIZE,ALL,,,DL2
MAT,M_NO3 $TYPE,2  $VMESH,10
MAT,M_NO2 $TYPE,2  $VMESH,9
RECT,-L1/2-F_L-LL,L1/2+F_L+LR,-L2/2-F_L-LH,UH+L2/2+F_L
asel,s,loc,z,0
aovlap,all
NSEL,S,LOC,Z,0,(H1+H2)*1.0001
ESLN
NUMMRG,NODE
KSEL,S,LOC,Z,0,(H1+H2)*1.0001
NUMMRG,KP
LSEL,S,LOC,X,(-L1/2-F_L-LL)*1.001,(-L1/2-F_L-LL)*0.999
LESIZE,ALL,,,DLL
LSEL,S,LOC,X,(L1/2+F_L+LR)*0.999,(L1/2+F_L+LR)*1.001
LESIZE,ALL,,,DLR
LSEL,S,LOC,Y,(-F_L-L2/2-LH)*1.001,(-F_L-L2/2-LH)*0.999
LESIZE,ALL,,,DLH
LSEL,S,LOC,Y,(UH+L2/2+F_L)*0.999,(UH+L2/2+F_L)*1.001
LESIZE,ALL,,,DUH
ASLL
MAT,M_NO4  $TYPE,1
R,R_NO4,R_V4  $REAL,R_NO4
AMESH,ALL
VSEL,S,LOC,Z,0,H1+H2
ASLV
ASEL,R,LOC,Z,0
AMESH,ALL
AGEN,2,ALL,,,,0
VSEL,S,LOC,Z,0,H1+H2
ASLV
ASEL,R,LOC,Z,0
ACLEAR,ALL
ALLS
/EOF
```

C* COMPONT.LIB**

```
C_RE3
*MSG,WARN,arg1
ASSEMBLE COMPONT Resistor with 3 Leads <- %C
CSYS,11
WPAVE
*ULIB,parts2,lib
*USE,RE3,arg1
WV1=(LL+L2)*cos(ROT0)-(LH-MY)*sin(ROT0)
WV2=(LL+L2)*sin(ROT0)+(LH-MY)*cos(ROT0)
CSYS,0
LOCAL,15,0,X0+WV1,Y0+WV2,Z0,ROT0
CSYS,11
VTRAN,15,1,23
LSEL,S,LOC,Z,0
ASLL
ASEL,R,MAT,,PWB
ATRAN,15,ALL
ALLS
VSEL,S,VOLU,,1,23
vclear,all
asel,s,area,,1,115
aclear,all
vdel,1,23
adel,1,115
ldel,1,173
kdel,1,87
!numcmp,kp
!numcmp,line
!numcmp,area
!numcmp,volu
/EOF

C_RE2
C*** Resistor with 2 Solder joint on side.
*MSG,WARN,arg1
ASSEMBLY COMPONT Resistor with 2 Leads <- %C
CSYS,11
WPAVE
*ULIB,parts2,lib
*USE,RE2,arg1
CSYS,0
LOCAL,15,0,X0,Y0,Z0,ROT0
CSYS,11
ATRAN,15,41,49,,,,1
VTRAN,15,1,7,,,,1
/EOF
```

```
TSOP_I
C*** TSOP with solder Joints.
C*** 1. Generate Block in cs-11, then move to cs-12
C*** 2. Generate J-lead in cs-11, then copy to cs-12 for multi-copies.
C*** 3. Generate Solder Joint in cs-11 then copy to each lead in cs-12.
C*** 4. Copy all the Volu to cs-0 (global location).
C*** Passed args are:'I_lead0','BLOCK0','SOLD_I0','PWB_I0'
*MSG,WARN,arg1,arg2,arg3,arg4
ASSEMBLE COMPONT TSOP w I-Leads <-%C, %C, %C, %C
CSYS,11
WPAVE
! Read data info. for block location.
! Lead and solder joint geo are needed
*ULIB,parts2,lib
*USE,BLOCK,arg2
WV0=4*(NX+NY)+NXC*NYC
*ULIB,data,lib
*USE,arg1
*USE,arg2
*USE,arg3
*USE,arg4
WV1=XYZ12+L1+L2+L2M+LL+R1+R2
WV2=XYZ12+L1+L2+L2M+LH+R1+R2
WV3=XYZ12+S_H+R2+H+R1
LOCAL,15,0,WV1,WV2,WV3
CSYS,11
ATRAN,15,1,WV0,,,,1
!Start I-Lead.
CSYS,11
WPAVE
*ULIB,parts2,lib
*USE,I_LEAD,arg1
LOCAL,15,0,XYZ12,XYZ12,XYZ12+S_H,,90
CSYS,11
ATRAN,15,1,5,,,,1
!copy to side (along y)
LR12=L1+L2+R1+R2
!Right-side.
*DO,I,1,NY,1
WV1=LL+L2M+LR12+2*MX+NX*(W+SX)-SX
WV2=LH+L2M+LR12+MY+(I-1)*(W+SY)
AGEN,2,1,5,,WV1,WV2,,,,0
*ENDDO
!Left side
LOCAL,15,0,XYZ12,XYZ12,XYZ12,180
CSYS,12
ATRAN,15,1,5,,,,1
```

```
*DO,I,1,NY-1,1
WV1=LL+L2M+LR12
WV2=W+LH+L2M+LR12+MY+(I-1)*(W+SY)
AGEN,2,1,5,,WV1,WV2,,,,0
*ENDDO
I=NY
WV1=LL+L2M+L2+L1+R1+R2
WV2=W+LH+L2M+LR12+MY+(I-1)*(W+SY)
*IF,LEADSIDE,EQ,2,THEN
 AGEN,2,1,5,,WV1,WV2,,,,1
*ELSE
 AGEN,2,1,5,,WV1,WV2,,,,0
*ENDIF
*IF,LEADSIDE,EQ,4,THEN
 LOCAL,15,0,XYZ12,XYZ12,XYZ12,90
 CSYS,12
 ATRAN,15,1,5,,,,1
 *DO,I,1,NX,1
  WV1=LL+L2M+LR12+MX+(I-1)*(W+SX)
  WV2=LH+L2M+L1+L2+R1+R2
  AGEN,2,1,5,,WV1,WV2,,,,0
 *ENDDO
 LOCAL,15,0,XYZ12,XYZ12,XYZ12,180
 CSYS,12
 ATRAN,15,1,5,,,,1
 *DO,I,1,NX-1,1
  WV1=W+LL+L2M+LR12+MX+(I-1)*(W+SX)
  WV2=LH+L2M+LR12+2*MY+NY*(W+SY)-SY
  AGEN,2,1,5,,WV1,WV2,,,,0
 *ENDDO
 I=NX
 WV1=W+LL+L2M+LR12+MX+(I-1)*(W+SX)
 WV2=LH+L2M+LR12+2*MY+NY*(W+SY)-SY
 AGEN,2,1,5,,WV1,WV2,,,,1
*ENDIF
!Start for Solder Joint
CSYS,11
WPAVE
*ULIB,parts2,lib
*USE,SOLD_I,arg1,arg3
LOCAL,15,0,XYZ12,XYZ12,XYZ12,,90
CSYS,11
VTRAN,15,1,,,,,1
!Right-side
*DO,I,1,NY,1
 WV11=LL+L2M+L2+L1+R1+R2+2*MX
 WV1=WV11+NX*(W+SX)-SX+L1+R1+R2-L2P
```

```
 WV11=LH+L2M+L2+L1+R1+R2+MY
 WV2=WV11+(I-1)*(W+SY)
VGEN,2,1,,,WV1,WV2,,,,0
*ENDDO
!Left-side
LOCAL,15,0,XYZ12,XYZ12,XYZ12,180
CSYS,12
VTRAN,15,1,,,,,1
*DO,I,1,NY-1,1
 WV1=LL+L2M+L2+L2P
 WV11=LH+L2M+L2+L1+R1+R2+MY
 WV2=WV11+(I-1)*(W+SY)+W
VGEN,2,1,,,WV1,WV2,,,,0
*ENDDO
I=NY
WV1=LL+L2M+L2+L2P
WV11=LH+L2M+L2+L1+R1+R2+MY
WV2=WV11+(I-1)*(W+SY)+W
*IF,LEADSIDE,EQ,2,THEN
 VGEN,2,1,,,WV1,WV2,,,,1
*ELSE
 VGEN,2,1,,,WV1,WV2,,,,0
*ENDIF
*IF,LEADSIDE,EQ,4,THEN
 LOCAL,15,0,XYZ12,XYZ12,XYZ12,90
 CSYS,12
 VTRAN,15,1,,,,,1
 *DO,I,1,NX,1
  WV11=LL+L2M+L2+L1+R1+R2+MX
  WV1=WV11+(I-1)*(W+SX)
  WV2=LH+L2M+L2+L2P
  VGEN,2,1,,,WV1,WV2,,,,0
 *ENDDO
 LOCAL,15,0,XYZ12,XYZ12,XYZ12,180
 CSYS,12
 VTRAN,15,1,,,,,1
 *DO,I,1,NX-1,1
  WV11=LL+L2M+L2+L1+R1+R2+MX
  WV1=WV11+(I-1)*(W+SX)+W
  WV11=LH+L2M+L1+L2+R1+R2+2*MY
  WV2=WV11+NY*(W+SY)-SY+L1+R1+R2-L2P
  VGEN,2,1,,,WV1,WV2,,,,0
 *ENDDO
 I=NX
  WV11=LL+L2M+L2+L1+R1+R2+MX
  WV1=WV11+(I-1)*(W+SX)+W
  WV11=LH+L2M+L1+L2+R1+R2+2*MY
```

```
  WV2=WV11+NY*(W+SY)-SY+L1+R1+R2-L2P
  VGEN,2,1,,,WV1,WV2,,,,1
*ENDIF
!Start Board Assembly.
 CSYS,11
 WPAVE
 *ULIB,parts2,lib
 *USE,PWB_I,arg1,arg2,arg3,arg4
 LOCAL,15,0,XYZ12+LL,XYZ12+LH,XYZ12
 CSYS,11
 ATRAN,15,1,4*(NX+NY)+NXC*NYC+16,,,,1
!Send Them to final global location
!Defined as X10,Y0,Z0,Rot0.
LOCAL,15,0,X0,Y0,Z0,ROT0
CSYS,12
VSEL,S,LOC,Z,0,S_H+R2
ALLS,BELOW
VTRAN,15,ALL,,,,,1
ALLS
LSEL,S,LOC,Z,-PWB_T,(S_H+R2+H+R1)*1.1
ASLL
ATRAN,15,ALL,,,,,1
ALLS
/EOF

TSOP_J
C*** TSOP of J-LEAD with solder Joints.
C*** 1. Generate Block in cs-11, then move to cs-12
C*** 2. Generate J-lead in cs-11, then copy to cs-12 for multi-copies.
C*** 3. Generate Solder Joint in cs-11 then copy to each lead in cs-12.
C*** 4. Copy all the Volu to cs-0 (global location).
C*** Passed args are:'J_lead0','BLOCK0','SOLD_J0','PWB_J0'
*MSG,WARN,arg1,arg2,arg3,arg4
ASSEMBLE COMPONT TSOP w J-Leads <- %C, %C, %C, %C
CSYS,11
WPAVE
!Create the BLOCk first.
*ULIB,parts2,lib
*USE,BLOCK,arg2
WV4=4*(NX+NY)+NXC*NYC
!Read data info. for block location.
! Lead and solder joint geo are needed
*ULIB,data,lib
*USE,arg1
*USE,arg2
*USE,arg3
*USE,arg4
```

```
WV1=XYZ12+LL+L2M+R1+L1
WV2=XYZ12+LH+L2M+R1+L1
WV3=XYZ12+S_H+R2+H+R1
LOCAL,15,0,WV1,WV2,WV3
CSYS,11
ATRAN,15,1,WV4,,,,1
!Start J-Lead creation.
CSYS,11
WPAVE
*ULIB,parts2,lib
*USE,J_LEAD,arg1
LOCAL,15,0,XYZ12,XYZ12,XYZ12+S_H,,90
CSYS,11
ATRAN,15,1,5,,,,1
!copy to side (along y)
!Right-side.
*DO,I,1,NY,1
WV1=LL+L2M+R1+L1+2*MX+NX*(W+SX)-SX
WV2=LH+L2M+R1+L1+MY+(I-1)*(W+SY)
AGEN,2,1,5,,WV1,WV2,,,,0
*ENDDO
!Left-Side.
LOCAL,15,0,XYZ12,XYZ12,XYZ12,180
CSYS,12
ATRAN,15,1,5,,,,1
*DO,I,1,NY-1,1
WV1=LL+L2M+R1+L1
WV2=LH+L2M+R1+L1+MY+(I-1)*(W+SY)+W
AGEN,2,1,5,,WV1,WV2,,,,0
*ENDDO
I=NY
WV1=LL+L2M+R1+L1
WV2=W+LH+L2M+R1+L1+MY+(I-1)*(W+SY)
*IF,LEADSIDE,EQ,2,THEN
 AGEN,2,1,5,,WV1,WV2,,,,1
*ELSE
 AGEN,2,1,5,,WV1,WV2,,,,0
*ENDIF
!For lower and upper side.
*IF,LEADSIDE,EQ,4,THEN
 LOCAL,15,0,XYZ12,XYZ12,XYZ12,90
 CSYS,12
 ATRAN,15,1,5,,,,1
 *DO,I,1,NX,1
  WV1=LL+L2M+R1+L1+MX+(I-1)*(W+SX)
  WV2=LH+L2M+R1+L1
   AGEN,2,1,5,,WV1,WV2,,,,0
```

```
 *ENDDO
 LOCAL,15,0,XYZ12,XYZ12,XYZ12,180
 CSYS,12
 ATRAN,15,1,5,,,,1
 *DO,I,1,NX-1,1
  WV1=W+LL+L2M+R1+L1+MX+(I-1)*(W+SX)
  WV2=LH+L2M+R1+L1+2*MY+NY*(W+SY)-SY
  AGEN,2,1,5,,WV1,WV2,,,,0
 *ENDDO
 I=NX
 WV1=W+LL+L2M+R1+L1+MX+(I-1)*(W+SX)
 WV2=LH+L2M+R1+L1+2*MY+NY*(W+SY)-SY
 AGEN,2,1,5,,WV1,WV2,,,,1
*ENDIF
!Start Solder Joint
CSYS,11
WPAVE
*ULIB,parts2,lib
*USE,SOLD_J,arg1,arg3
LOCAL,15,0,XYZ12,XYZ12,XYZ12,,90
CSYS,11
VTRAN,15,1,,,,,1
!Right-side.
*DO,I,1,NY,1
 WV11=LL+L2M+R1+L1+2*MX+NX*(W+SX)-SX
 WV1=WV11+L1+R1-2*R2-L2P
 WV2=LH+L2M+R1+L1+MY+(I-1)*(W+SY)
 VGEN,2,1,,,WV1,WV2,,,,0
*ENDDO
!Left-side.
LOCAL,15,0,XYZ12,XYZ12,XYZ12,180
CSYS,12
VTRAN,15,1,,,,,1
*DO,I,1,NY-1,1
 WV1=LL+L2M+2*R2+L2P
 WV2=W+LH+L2M+R1+L1+MY+(I-1)*(W+SY)
 VGEN,2,1,,,WV1,WV2,,,,0
*ENDDO
I=NY
WV1=LL+L2M+2*R2+L2P
WV2=W+LH+L2M+R1+L1+MY+(I-1)*(W+SY)
*IF,LEADSIDE,EQ,2,THEN
 VGEN,2,1,,,WV1,WV2,,,,1
*ELSE
 VGEN,2,1,,,WV1,WV2,,,,0
*ENDIF
*IF,LEADSIDE,EQ,4,THEN
```

```
 LOCAL,15,0,XYZ12,XYZ12,XYZ12,90
 CSYS,12
 VTRAN,15,1,,,,,1
 *DO,I,1,NX,1
  WV1=LL+L2M+R1+L1+MX+(I-1)*(W+SX)
  WV2=LH+L2M+2*R2+L2P
  VGEN,2,1,,,WV1,WV2,,,,0
 *ENDDO
  LOCAL,15,0,XYZ12,XYZ12,XYZ12,180
 CSYS,12
 VTRAN,15,1,,,,,1
 *DO,I,1,NX-1,1
  WV1=LL+L2M+R1+L1+MX+(I-1)*(W+SX)+W
  WV11=LH+L2M+R1+L1+2*MY+NY*(W+SY)-SY
  WV2=WV11+L1+R1-2*R2-L2P
  VGEN,2,1,,,WV1,WV2,,,,0
 *ENDDO
 I=NX
 WV1=LL+L2M+R1+L1+MX+(I-1)*(W+SX)+W
 WV11=LH+L2M+R1+L1+2*MY+NY*(W+SY)-SY
 WV2=WV11+L1+R1-2*R2-L2P
 VGEN,2,1,,,WV1,WV2,,,,1
*ENDIF
!Start Board Assembly.
 CSYS,11
 WPAVE
 *ULIB,parts2,lib
 *USE,PWB_J,arg1,arg2,arg3,arg4
 LOCAL,15,0,XYZ12+LL,XYZ12+LH,XYZ12
 CSYS,11
 ATRAN,15,1,4*(NX+NY)+NXC*NYC+16,,,,1
!Send Them to final global location
!Defined as X10,Y0,Z0,Rot0.
LOCAL,15,0,X0,Y0,Z0,ROT0
CSYS,12
VSEL,S,LOC,Z,0,S_H+R2
ALLS,BELOW
VTRAN,15,ALL,,,,,1
ALLS
LSEL,S,LOC,Z,-PWB_T,(S_H+R2+H+R1)*1.1
ASLL
ATRAN,15,ALL,,,,,1
/EOF

C_FCOB
C*** Move The FCOB created in PARTS2.lib to Final Location.
*MSG,WARN,arg1
```

```
ASSEMBLE COMPONT Flip-Chip on Board <- %C
CSYS,11
WPAVE
*ULIB,parts2,lib
*USE,FCOB,arg1
WV1=(L1/2+F_L+LL)*cos(ROT0)-(L2/2+F_L+LH)*sin(ROT0)
WV2=(L1/2+F_L+LL)*sin(ROT0)+(L2/2+F_L+LH)*cos(ROT0)
LOCAL,15,0,X0+WV1,Y0+WV2,Z0,ROT0
!LOCAL,15,0,X0+L1/2+F_L+LL,Y0+L2/2+F_L+LH,Z0,ROT0
CSYS,11
LSEL,S,LOC,Z,0
ASLL
VSEL,S,LOC,Z,0,H1+H2
ASLV,U
ATRAN,15,ALL
LSEL,S,LOC,Z,0
ASLL
VSEL,S,LOC,Z,0,H1+H2
ASLV,U
ACLEAR,ALL
ADEL,ALL
VSEL,S,LOC,Z,0,H1+H2
ASLV
LSLA
LSEL,INVE
LSEL,R,LOC,Z,0
LDEL,ALL
VSEL,S,LOC,Z,0,H1+H2
VTRAN,15,ALL,,,,,1
ALLS
/EOF
```

Part 3. Sample Data Input File:

```
BLOCK1
C*** For a TSOP with 4 side Leads.
C*** Define a Plastic Block for a I or J Lead TSOP
C*** REAL 11 is the thickness of block.
LEADSIDE=4
W=12  $DW=2
MX=18   $DMX=2
MY=18   $DMY=2
NX=10
NY=10
NXC=7
NYC=7
SX=12   $DSX=1
```

```
SY=12   $DSY=1
M_NO1=PLAS1  $R_NO1=11   $R_V1=21
/EOF

I_LEAD1
C*** Define the geometry of a Gull-Lead -> I-lead.
L1=8      $DL1=2
L2=8      $DL2=3
 H=15      $ DH=2
R1=5   $DR1=3
R2=5     $DR2=3
W=12       $DW=2
T=1
M_NO1=LEAD1 $R_NO1=12  $R_V1=T  !R_NO1 here is unique.
                        !Start from 11 for nonglobal R type definition.
/EOF

PWB_I1
C*** Define a Board Geo. corresponding to a I-lead Component.
C*** PWB_I0 OVERWRITE BLOCK0 DATA.
X0=0  $Y0=380   $Z0=0   $ROT0=0
LL=40   $LR=40   $LH=38   $UH=38
DLL=38  $DLR=50  $DLH=45 $DUH=36
D1=7    $D2=7    $D3=7   $D4=7
DMX=3   $DMY=3   $DSX=1   $DSY=1
!DMX=MX+L1=L2P, These Par. are for PWB board patch.
NXC=9   $NYC=9  !Overwrite the NXC and NYC in BLOCK.
M_NO1=PWB    $R_NO1=PWB_R    $R_V1=PWB_T
/EOF

SOLD_I1
C*** Solder joint Geometry for I-lead.

L2P=R2+3  $L2M=4 !Solder joint extension above a Lead.
S_H=2.5 !Solder joint height of coplanarity.
DS_H=3
D_ratio=-2
M_NO1=TRASH    $R_NO1=TRASH_R    $R_V1=TRASH_T
M_NO2=SOLDER
/EOF


FCOB1
C*** Define a DCA geo. and final location.
C*** DCA include Die ENCAP and Fr4 board.
X0=0   $Y0=0  $Z0=0   $ROT0=0
L1=150  $L2=150
```

```
DL1=10  $DL2=10
H1=5    $H2=25
DH1=2   $DH2=3
F_L=35  $R=50
DF_L=4  $DR=7 $DRO=4
B_L1=20 $B_L2=30
LL=92  $LH=80   $LR=92   $UH=80
DLL=26 $DLH=26  $DLR=36  $DUH=45
M_NO1=TRASH  $R_NO1=TRASH_R  $R_V1=TRASH_T
M_NO2=EPOXY
M_NO3=SILICON
M_NO4=PWB    $R_NO4=PWB_R    $R_V4=PWB_T
/EOF

BLOCK2
C*** For a TSOP with 4 side Leads.
C*** Define a Plastic Block for a I or J Lead TSOP
C*** REAL 11 is the thickness of block.
LEADSIDE=4
W=12  $DW=2
MX=20   $DMX=2
MY=20   $DMY=2
NX=8
NY=8
NXC=6
NYC=6
SX=13   $DSX=1
SY=13   $DSY=1
M_NO1=PLAS1  $R_NO1=13   $R_V1=21
/EOF

J_LEAD2
C*** Define geometry of a J-lead.
W=12   $DW=2
L1=6  $DL1=2
R1=4  $DR1=3
H=8   $DH=3
R2=5 $DR2=3   !DR2*2= Total div. of lower J-lead div.
M_NO1=LEAD1  $R_NO1=14  $R_V1=0.5  !R_No1=12 is local deinfed
                        !It should be unique!!!
/EOF

SOLD_J2
C*** Define a Solder joint connection for a J-LEAD.
L2P=3.
L2M=4.
S_H=2.5. !Solder joint height of coplanarity.
```

```
DS_H=3
D_ratio=-2
M_NO1=TRASH    $R_NO1=TRASH_R    $R_V1=TRASH_T
M_NO2=SOLDER
/EOF

PWB_J2
C*** Define a Board Geo. corresponding to a I-lead Component.
C*** PWB_I0 OVERWRITE BLOCK0 DATA.
X0=404  $Y0=0   $Z0=0   $ROT0=0
LL=52   $LR=53   $LH=62   $UH=63
DLL=36  $DLR=44  $DLH=36 $DUH=40
D1=7    $D2=7    $D3=7   $D4=7
DMX=3   $DMY=3   $DSX=1   $DSY=1
!DMX=MX+L1=L2P, These Par. are for PWB board patch.
NXC=8   $NYC=8  !Overwrite the NXC and NYC in BLOCK.
M_NO1=PWB    $R_NO1=PWB_R    $R_V1=PWB_T
/EOF

RE2_1
C***
X0=404  $Y0=380+160  $Z0=0  $ROT0=0
H1=2  $H2=12
DH1=2 $DH2=4
L1=4  $L2=12  $L3=20
DL1=2 $DL2=DH1+DH2 $DL3=4
W=12   $R=20
DW=3
LL=54  $LH=34  $LR=54  $UH=34
DLL=15 $DLH=10 $DLR=15 $DUH=10
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/EOF

RE2_2
C***
X0=404+120  $Y0=380+160  $Z0=0  $ROT0=0
H1=2  $H2=12
DH1=2 $DH2=4
L1=4  $L2=12  $L3=20
DL1=2 $DL2=DH1+DH2 $DL3=4

W=12   $R=20
DW=3
```

```
LL=54  $LH=34  $LR=54  $UH=34
DLL=15 $DLH=10 $DLR=15 $DUH=12
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/EOF


RE2_3
C***
X0=404+240  $Y0=380+160  $Z0=0  $ROT0=0
H1=3  $H2=22
DH1=2 $DH2=4
L1=8  $L2=16  $L3=34
DL1=2 $DL2=DH1+DH2 $DL3=4
W=20   $R=45
DW=3
LL=50  $LH=19  $LR=50  $UH=19
DLL=15 $DLH=10 $DLR=12 $DUH=12
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/EOF

RE2_4
C***
X0=404  $Y0=380+400  $Z0=0  $ROT0=-90
H1=3  $H2=22
DH1=2 $DH2=4
L1=8  $L2=16  $L3=34
DL1=2 $DL2=DH1+DH2 $DL3=4
W=20   $R=45
DW=3
LL=50  $LH=19  $LR=50  $UH=19
DLL=10 $DLH=15 $DLR=10 $DUH=15
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/EOF

RE2_5
C***
X0=404+120  $Y0=380+400  $Z0=0  $ROT0=-90
H1=2  $H2=12
```

```
DH1=2 $DH2=4
L1=4  $L2=12  $L3=20
DL1=2 $DL2=DH1+DH2 $DL3=4
W=12   $R=20
DW=3

LL=54  $LH=34  $LR=54  $UH=34
DLL=10 $DLH=15 $DLR=12 $DUH=15
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/EOF


RE2_6
C***
X0=404+240  $Y0=380+400  $Z0=0  $ROT0=-90
H1=2  $H2=12
DH1=2 $DH2=4
L1=4  $L2=12  $L3=20
DL1=2 $DL2=DH1+DH2 $DL3=4
W=12   $R=20
DW=3
LL=54  $LH=34  $LR=54  $UH=34
DLL=10 $DLH=15 $DLR=12 $DUH=12
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/EOF

RE3_1
C*** Define the a Resistor with 3 Leads.
C*** One on left side, two on right side.
C*** Rotate the direction for different application.
C*** THese should be global variables.
C*** TRASH,TRASH_R, TRASH_T, SOLDER, PLAS1,PWB, PWB_T,PWB_R
 ! Define the final location of the Re. Component.
 X0=404  $Y0=380  $Z0=0  $ROT0=0
H1=4  $H2=10  $H3=10          !H1->Re'height to PWB, h2-> solder height on Re.
                    !H3->Re's height above solder.
DH1=2 $DH2=4 $DH3=2         !DH1+DH2-> has to be EVEN Number.
L1=30/2  $L2=20              !L1->re's width/2 L2-> solder base length .
DL1=4 $DL2=DH1+DH2
MY=14  $W=15  $SY=18           !MY->Lead y-mrgine to lower side
                    !W ->solder joint width, SY-> y-seperation.
```

```
DMY=2 $DW=2 $DSY=1
R=35
DR=DL2
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
! For PWB associated with this Re.
LL=55  $LH=56  $LR=55  $UH=56
DLL=20 $DLH=20 $DLR=15 $DUH=15
D_1=8 $D_2=8 $D_3=8 $D_4=8
DL11=4 ! Center line div. for PWB of Re.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/eof

RE3_2
C*** Define the a Resistor with 3 Leads.
C*** One on left side, two on right side.
C*** Rotate the direction for different application.
C*** THese should be global variables.
C*** TRASH,TRASH_R, TRASH_T, SOLDER, PLAS1,PWB, PWB_T,PWB_R
 ! Define the final location of the Re. Component.
 X0=404+180  $Y0=380+160  $Z0=0  $ROT0=-90
H1=4  $H2=10  $H3=10          !H1->Re'height to PWB, h2-> solder height on Re.
                      !H3->Re's height above solder.
DH1=2 $DH2=4 $DH3=2         !DH1+DH2-> has to be EVEN Number.
L1=30/2  $L2=20              !L1->re's width/2 L2-> solder base length .
DL1=4 $DL2=DH1+DH2
MY=14  $W=15  $SY=18          !MY->Lead y-mrgine to lower side
                      !W ->solder joint width, SY-> y-seperation.
DMY=2 $DW=2 $DSY=1
R=35
DR=DL2
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
! For PWB associated with this Re.
LL=45  $LH=66  $LR=45  $UH=66
DLL=15 $DLH=15 $DLR=20 $DUH=16
D_1=8 $D_2=8 $D_3=8 $D_4=8
DL11=4 ! Center line div. for PWB of Re.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/eof


BLOCK3
C*** For a TSOP with 4 side Leads.
C*** Define a Plastic Block for a I or J Lead TSOP
C*** REAL 11 is the thickness of block.
LEADSIDE=2
```

```
W=12  $DW=2
MX=18   $DMX=2
MY=18   $DMY=2
NX=6
NY=8
NXC=5
NYC=8
SX=12   $DSX=1
SY=15   $DSY=1
M_NO1=PLAS1  $R_NO1=11   $R_V1=21
/EOF

I_LEAD3
C*** Define the geometry of a Gull-Lead -> I-lead.
L1=8      $DL1=2
L2=8      $DL2=3
 H=15      $ DH=2
R1=5   $DR1=3
R2=5     $DR2=3
W=12       $DW=2
T=1
M_NO1=LEAD1 $R_NO1=12  $R_V1=T  !R_NO1 here is unique.
                        !Start from 11 for nonglobal R type definition.
/EOF

PWB_I3
C*** Define a Board Geo. corresponding to a I-lead Component.
C*** PWB_I0 OVERWRITE BLOCK0 DATA.
X0=404+360  $Y0=380   $Z0=0   $ROT0=-90
!LL=86   $LR=86   $LH=43   $UH=40
!DLL=44  $DLR=38  $DLH=45 $DUH=48
LL=76   $LR=76   $LH=53   $UH=50
DLL=48  $DLR=45  $DLH=44 $DUH=38
D1=9    $D2=9    $D3=9   $D4=9
DMX=3   $DMY=3   $DSX=1   $DSY=1
!DMX=MX+L1=L2P, These Par. are for PWB board patch.
NXC=6   $NYC=8  !Overwrite the NXC and NYC in BLOCK.
M_NO1=PWB    $R_NO1=PWB_R    $R_V1=PWB_T

/EOF

SOLD_I3
C*** Solder joint Geometry for I-lead.
L2P=R2+3  $L2M=4 !Solder joint extension above a Lead.
S_H=2.5 !Solder joint height of coplanarity.
DS_H=3
D_ratio=-1.5
```

```
M_NO1=TRASH    $R_NO1=TRASH_R    $R_V1=TRASH_T
M_NO2=SOLDER
/EOF

FCOB2
C*** Define a DCA geo. and final location.
C*** DCA include Die ENCAP and Fr4 board.
X0=764   $Y0=380+400  $Z0=0   $ROT0=-90
L1=220  $L2=140
DL1=14  $DL2=10
H1=5    $H2=33
DH1=2   $DH2=4
F_L=40  $R=50
DF_L=4  $DR=7 $DRO=4
B_L1=20 $B_L2=30
!LL=50  $LH=90   $LR=50   $UH=90
!DLL=40 $DLH=48  $DLR=30  $DUH=30
LL=50  $LH=90   $LR=50   $UH=90
DLL=30 $DLH=40  $DLR=48  $DUH=30
M_NO1=TRASH  $R_NO1=TRASH_R  $R_V1=TRASH_T
M_NO2=EPOXY
M_NO3=SILICON
M_NO4=PWB    $R_NO4=PWB_R    $R_V4=PWB_T
/EOF
```

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VITA

On March 15, 1969, Wen Xu Zhou was born in Suzhou, JiangSu Provence in People's Republic of China. A few month later, he moved with his parents to Beijing the capital of China. It is that place where he grow up, and had witnessed significant changes since mid 1970s, include unforgettable culture revolution, remarkable economic reforms and society transition, and the outrageous turmoil on Tian-an-men Square. In 1992, he marrid Hong Yin, whom he knew from mid-school in Beijing.

The author had never been a good student, but he has been blessed to advance to graduated shool. He graduated in 1987 from *August-First* high school in Beijing. He spent about three-year studies in physics in Beijing Normal University, but did not get a Bacelar degree. In 1992, He earned his Master degree with thesis in Mechanical Engineering from Georgia Institute of Technology. Four years later, He received a Doctorate degree in Mechancial Engineering.

Apendix A

List of Program

The code used in the thesis are list in this Appendix. The program consists three main parts: 1) MAIN input program, 2) MACRO(subroutine) program, and 3) data file. The programs and comments are listed as follows:

Part 1. MAIN input program:

```
/prep7          ! start pre-processor.
et,2,45         ! two element types are used: Solid-45 and Shell-63.
et,1,63
pre_def         ! predefinitions that are specified in PRE_DEF macro.
csys,11
WPAVE       ! Specify local coodinate system.
*MSG,WARN
ASSEMBLE FCOB-01
*ULIB,compont,lib             ! the program format for creating a component.
*USE,C_FCOB,'FCOB1'    ! The *UIB specify  component file, which is component.lib
                        ! The *USE specify the component to be used, and the
                            !  geometry data file associated with this component.
                            ! C_FCOB is the component type, and the FCOB1 is the
                            geometry data block.
*ULIB,compont,lib
*USE,TSOP_I,'I_lead1','BLOCK1','SOLD_I1','PWB_I1'
! Similar to C_FOB, A TSOP_I is the component type and I_lead1, BLOCK1, and SOLD_I1 are
its MGPs.
*ULIB,compont,lib
! TSOP_J means a component with J-leads on its sode.
*USE,TSOP_J,'J_lead2','BLOCK2','SOLD_J2','PWB_J2'
*ULIB,compont,lib
! C_RE3 applys to a passive component with three solder joints.
*USE,C_RE3,'RE3_1'
```

```
*ULIB,compont,lib
*USE,C_RE3,'RE3_2'
*ULIB,compont,lib
! C_RE2 applys to a passive component with 2 solder joints.
*USE,C_RE2,'RE2_1'
*ULIB,compont,lib
*USE,C_RE2,'RE2_2'
*ULIB,compont,lib
*USE,C_RE2,'RE2_3'
*ULIB,compont,lib
*USE,C_RE2,'RE2_4'
*ULIB,compont,lib
*USE,C_RE2,'RE2_5'
*ULIB,compont,lib
*USE,C_RE2,'RE2_6'
*ULIB,compont,lib
*USE,TSOP_I,'I_lead3','BLOCK3','SOLD_I3','PWB_I3'
*ULIB,compont,lib
*USE,C_FCOB,'FCOB2'
!KSEL,S,LOC,X,-300,400
! the following 8 lines are used as book keeping  commands.
!KDEL,ALL
ALLS
CSYS,0
WPAVE
alls
aslv
aclear,all
alls

!DEFINE ELEMENTS COLOR.
/plopt,defa
/plott,info,off
ESEL,S,MAT,,SILICON
/COLOR,elem,BMAG
ESEL,S,MAT,,EPOXY
/COLOR,ELEM,ORAN
ESEL,S,MAT,,PLAS1
/COLOR,ELEM,GREEN
ESEL,S,MAT,,SOLDER
/COLOR,ELEM,RED
ESEL,S,MAT,,LEAD1
/COLOR,ELEM,BLUE
! Merge all the coincident items, include key points, element, and constraints.
ALLS
KSLL
KSEL,INVE
```

```
KDEL,ALL
ALLS
NUMMRG,NODE,2e-4
NUMMRG,KP
NUMMRG,ELEM
NUMMRG,CE
! Desired analysis type starts after this line.
```

Part 2. Component Library Input File:

```
RE3
C*** Generate a resistor with 2 and 3 solder joints.
C*** RE3 Create KP= 87, LINE=173, AREA=115, VOLU=23
NUM_OFF,90,175,115,25
*ULIB,data,lib
*USE,arg1
WV1=2*(MY+W)+SY
WV2=(WV1-W)/2/2
k,1,0,,H1
k,2,L1,,H1
k,3,2*L1,,H1
k,4,0,WV2,h1
k,5,L1,WV1/5,h1
k,6,2*L1,MY,h1
k,7,0,2*WV2,h1
k,8,L1,WV1/5*2,h1
k,9,2*L1,MY+W,h1
k,10,0,2*WV2+W,h1
k,11,L1,WV1/5*3,h1
k,12,2*L1,MY+W+SY,h1
k,13,0,WV1-WV2,h1
k,14,L1,WV1/5*4,h1
k,15,2*L1,MY+W+SY+W,h1
k,16,0,WV1,h1
k,17,L1,WV1,h1
k,18,2*L1,WV1,h1
l,1,4
*repeat,5,3,3
l,3,6
*repeat,5,3,3
k,19,2*L1,MY
k,20,2*L1+L2,MY
k,21,2*L1,MY,H1+H2
k,22,2*L1+L2,MY,H1+H2
larc,21,20,22,R
k,23,2*L1,MY+W+SY
```

```
k,24,2*L1+L2,MY+W+SY
k,25,2*L1,MY+W+SY,H1+H2
k,26,2*L1+L2,MY+W+SY,H1+H2
larc,25,24,26,R
k,27,,WV2*2
k,28,-L2,WV2*2
k,29,,WV2*2,H1+H2
k,30,-L2,WV2*2,H1+H2
larc,28,29,30,R
a,6,19,20,21
a,12,23,24,25
a,7,29,28,27
!Define line division for solder profile areas.
 lsel,s,line,,14
 lsel,a,line,,17
 lsel,a,line,,22
 lesize,all,,,DH1
 lsel,s,line,,15
 lsel,a,line,,18
 lsel,a,line,,21
 lesize,all,,,DL2
 lsel,s,line,,16
 lsel,a,line,,19
 lsel,a,line,,20
 lesize,all,,,DH2
 alls
 lccat,14,16
 lccat,17,19
 lccat,20,22
 TYPE,1
 MAT,M_NO1
 R,R_NO1,RV1
 ESHAPE,2
 AMESH,1,3
 a,1,2,5,4
 *repeat,5,3,3,3,3
 a,2,3,6,5
 *repeat,5,3,3,3,3
 !start line div. on Areas.
 lsel,s,loc,x,L1*0.1,L1*0.9
 lsel,a,loc,x,L1*1.1,L1*1.9
 lesize,all,,,DL1
 lsel,s,line,,1
 lsel,a,line,,5
 lsel,a,line,,6
 lsel,a,line,,10
 lesize,all,,,DMY
```

```
 lsel,s,line,,2,4
 lsel,a,line,,7,9
 lesize,all,,,DW
 alls
 AMESH,4,13
!Start ext to Re block.
 LDEL,23,25
 MAT,M_NO2  ! for solder fillet.
 TYPE,2
 ESIZE,,DW
 VEXT,1,3,,,W
 MAT,M_NO3  ! for Re block.
 TYPE,2
 ESIZE,,DH2
 VEXT,4,13,,,,H2
 ASEL,S,LOC,Z,H1+H2
 TYPE,1
 MAT,M_NO1 $R,R_NO1,R_V1
 AMESH,ALL
 TYPE,2 $MAT,M_NO3
 ESIZE,,DH3
 VEXT,ALL,,,,,H3
k,79  ! NO USE SCRATCH POINT.
k,80,-L2,MY
k,81,,MY
k,82,-L2,MY+2*W+SY
k,83,,MY+2*W+SY
k,84,-(L2+LL),MY-LH
k,85,2*L1+L2+LR,MY-LH
k,86,2*L1+L2+LR,MY+2*W+SY+UH
k,87,-(L2+LL),MY+2*W+SY+UH
a,80,81,27,28
a,81,19,33,27
a,27,33,23,39
a,33,34,24,23
a,42,39,83,82
a,39,23,37,83
a,84,85,20,19,81,80
a,85,86,38,24,34,20
a,82,83,37,38,86,87
a,84,80,28,42,82,87
a,19,20,34,33
a,23,24,38,37
a,28,27,39,42
! Line div. for PWB.
 lsel,s,line,,166
 lesize,all,,,DLH
```

```
 lsel,s,line,,169
 lesize,all,,,DLR
 lsel,s,line,,171
 lesize,all,,,DUH
 lsel,s,line,,173
 lesize,all,,,DLL
 lsel,s,line,,168
 lesize,all,,,D_1
 lsel,s,line,,167
 lesize,all,,,D_2
 lsel,s,line,,170
 lesize,all,,,D_3
 lsel,s,line,,172
 lesize,all,,,D_4
 lsel,s,line,,157,158
 lsel,a,line,,160,165,5
 lesize,all,,,DL11
 MAT,M_NO4 $TYPE,1 $R,R_NO4,R_V4
 AMESH,104,105
 AMESH,108
 AMESH,103
 AMESH,106
 AMESH,107
 AMESH,113,115
 ESHAPE, $ AMESH,109,112
 ALLS
/eof


RE2
C*** Generate a RESISTOR with 2-solder JOINTS on Side
C*** Create kp=63, line=96, area=49, volu=7
NUM_OFF,63,96,49,7
*ULIB,data,lib
*USE,arg1
!Generate halp of the Solder fillet, then copy.
k,1
k,2,L1
k,3,L1+L2
K,4,,H1
k,5,L1,H1
K,6,,H1+H2
K,7,L1,H1+H2
k,8,L1+L2,H1+H2
larc,7,3,8,R
a,1,2,5,4
a,2,3,7,5
```

```
a,4,5,7,6
!Start line div. control.
lsel,s,loc,x,L1*0.1,L1*0.9
LESIZE,ALL,,,DL1
LSEL,S,LINE,,7,9,2
LESIZE,ALL,,,DH2
LSEL,S,LINE,,3,5,2
LESIZE,ALL,,,DH1
ALLS
LCCAT,3,7
MAT,M_NO1
TYPE,1 $ESHAPE,2
R,R_NO1,R_V1
AMESH,1,3,2
AMESH,2
LDEL,10
ESIZE,,DW
TYPE,2
MAT,M_NO2
VEXT,1,2,,,,-W
MAT,M_NO3
VEXT,3,,,,,-W
!Generate Center Block.
BLOCK,-L3,0,H1,H1+H2,-W,0
LSEL,S,LINE,,39,42
LESIZE,ALL,,,DW
LSEL,S,LINE,,31,33,2
LSEL,A,LINE,,36,38,2
LESIZE,ALL,,,DH2
LSEL,S,LINE,,32,34,2
LSEL,A,LINE,,35,37,2
LESIZE,ALL,,,DL3,-3
TYPE,2
MAT,M_NO3
VMESH,4
ALLS
!COPY to another side.
LOCAL,15,0,XYZ11-L3,XYZ11,XYZ11-W,,,180
CSYS,11
!VTRAN,15,1,3,,,,1
VTRAN,15,1,3
LOCAL,15,0,XYZ11+W+LL,XYZ11+L3+L2+L1+LH,XYZ11,90,90
CSYS,11
VTRAN,15,1,7,,,,1
!Create AREA of PWB
 CSYS,11
 k,48,
```

```
k,49,LL+W+LR
k,50,LL+W+LR,LH+2*(L1+L2)+L3+UH
k,51,0,LH+2*(L1+L2)+L3+UH
k,52,LL,LH
k,53,LL,LH+L2
k,54,LL,LH+L1+L2
k,55,LL,LH+L1+L2+L3
k,56,LL,LH+L1+L2+L3+L1
k,57,LL,LH+L1+L2+L3+L1+L2
k,58,LL+W,LH
k,59,LL+W,LH+L2
k,60,LL+W,LH+L1+L2
k,61,LL+W,LH+L1+L2+L3
k,62,LL+W,LH+L1+L2+L3+L1
k,63,LL+W,LH+L1+L2+L3+L1+L2
a,48,52,53,54,55,56,57,51
a,48,49,58,52
a,58,49,50,63,62,61,60,59
a,63,50,51,57
a,52,58,59,53
*REPEAT,5,1,1,1,1
LESIZE,73,,,D1
LESIZE,82,,,D2
LESIZE,85,,,D3
LESIZE,79,,,D4
LESIZE,80,,,DLL
LESIZE,81,,,DLH
LESIZE,84,,,DLR
LESIZE,91,,,DUH
LSEL,S,LINE,,74,90,16
LSEL,A,LINE,,78,86,8
LESIZE,ALL,,,DL2
LSEL,S,LINE,,75,89,14
LSEL,A,LINE,,77,87,10
LESIZE,ALL,,,DL1
LSEL,S,LINE,,76,88,12
LESIZE,ALL,,,DL3*0.9
LSEL,S,LOC,X,LL*1.005,LL+W*0.99
LSEL,R,LOC,Y,LH*0.99,LH+2*(L1+L2)+L3-L2*0.001
LSEL,R,LOC,Z,0
LESIZE,ALL,,,DW
ALLS
MAT,M_NO4
TYPE,1
R,R_NO4,R_V4
ESHAPE,2
AMESH,45,49
```

```
 ESHAPE,
 AMESH,41,44
/eof

I_LEAD
C*** This is 3D Shell Model for a I-Lead
*ULIB,data,lib
*USE,arg1
NUM_OFF,16,18,5,0
k,1,,R2+H+R1
k,2,L1,R2+H+R1
k,3,L1+R1,R2+H
k,4,L1+R1,R2
k,5,L1+R1+R2
k,6,L1+R1+R2+L2
k,7,L1,R2+H
k,8,L1+R1+R2,R2
k,9,,R2+H+R1,-W
l,1,2
LARC,3,2,7,R1
l,3,4
LARC,4,5,8,R2
l,5,6
l,1,9
ADRAG,1,2,3,4,5,,6
LESIZE,1,,,DL1
LESIZE,2,,,DR1
LESIZE,3,,,DH
LESIZE,4,,,DR2
LESIZE,5,,,DL2
LSEL,S,LOC,Z,-W*0.9,-W*0.1
LESIZE,ALL,,,DW
MAT,M_NO1
TYPE,1
R,R_NO1,R_V1
REAL,R_NO1
ESHAPE,2
AMESH,1,5
LDEL,6
ALLS
/EOF


BLOCK
C*** Define a Block
C*** This Lib. Fun Generate Volu=0
```

```
C***                AREA=4*(NX+NY)+NXC*NYC
C***                LINE=4*AREA
C***                KP=4*AREA
*ULIB,data,lib
*USE,arg1
WV1=4*(NX+NY)+NXC*NYC
NUM_OFF,4*WV1,4*WV1,WV1,0
! Lower Side area creation.
RECT,0,MX,0,MY
WPOFF,MX
*DO,I,1,NX-1,1
 RECT,0,W,0,MY
 WPOFF,W
 RECT,0,SX,0,MY
 WPOFF,SX
*ENDDO
RECT,0,W,0,MY
WPAVE
WPOFF,,MY
*DO,I,1,NY-1,1
 RECT,0,MX,0,W
 WPOFF,,W
 RECT,0,MX,0,SY
 WPOFF,,SY
*ENDDO
 RECT,0,MX,0,W
WPAVE
!Line div for lwoer and left side.
LSEL,S,LOC,Y,MY*0.1,MY*0.9
LESIZE,ALL,,,DMY
LSEL,S,LOC,X,MX*0.1,MX*0.9
LESIZE,ALL,,,DMX
*DO,I,1,NX-1,1
WV1=MX+(I-1)*(W+SX)
LSEL,S,LOC,X,WV1+W*0.01,WV1+W*0.99
LESIZE,ALL,,,DW
LSEL,S,LOC,X,WV1+W+SX*0.01,WV1+W+SX*0.99
LESIZE,ALL,,,DSX
*ENDDO
I=NX
WV1=MX+(I-1)*(W+SX)
LSEL,S,LOC,X,WV1+W*0.01,WV1+W*0.99
LESIZE,ALL,,,DW
*DO,I,1,NY-1,1
WV1=MY+(I-1)*(W+SY)
LSEL,S,LOC,Y,WV1+W*0.01,WV1+W*0.99
LESIZE,ALL,,,DW
```

```
LSEL,S,LOC,Y,WV1+W+SY*0.01,WV1+W+SY*0.99
LESIZE,ALL,,,DSY
*ENDDO
I=NY
WV1=MY+(I-1)*(W+SY)
LSEL,S,LOC,Y,WV1+W*0.01,WV1+W*0.99
LESIZE,ALL,,,DW
ALLS
ASEL,S,LOC,Y,0,MY
LOCAL,15,0,XYZ11,XYZ11+MY+(NY-1)*(W+SY)+W,XYZ11
CSYS,11
ATRAN,15,ALL
ASEL,S,LOC,X,0,MX
LOCAL,15,0,XYZ11+MX+(NX-1)*(W+SX)+W,XYZ11,XYZ11
CSYS,11
ATRAN,15,ALL
WPAVE
WV1=(NX*(W+SX)-SX)/NXC
WV2=(NY*(W+SY)-SY)/NYC
*DO,I,1,NXC,1
*DO,J,1,NYC,1
 WPOFF,MX+(I-1)*WV1,MY+(J-1)*WV2
 RECT,0,WV1,0,WV2
 WPAVE
*ENDDO
*ENDDO
ASEL,S,LOC,X,MX,MX+NX*(W+SX)-SX
ASEL,R,LOC,Y,MY,MY+NY*(W+SY)-SY
LSLA
LESIZE,ALL,,,1
ALLS
TYPE,1
MAT,M_NO1
R,R_NO1,R_V1
REAL,R_NO1
AMESH,1,4*(NX+NY)+NXC*NYC
ALLS
*DO,I,1,NXC,1
 ASEL,S,LOC,X,MX+(I-1)*WV1,MX+I*WV1
 ASEL,R,LOC,Y,MY,MY+WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,MY
 NSEL,R,LOC,X,MX+(I-1)*WV1,MX+I*WV1
 CEINTF
*ENDDO
```

```
ALLS
*DO,I,1,NXC,1
 ASEL,S,LOC,X,MX+(I-1)*WV1,MX+I*WV1
 ASEL,R,LOC,Y,MY+(NYC-1)*WV2,MY+NYC*WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,MY+NYC*WV2
 NSEL,R,LOC,X,MX+(I-1)*WV1,MX+I*WV1
 CEINTF
*ENDDO
ALLS
*DO,I,1,NYC
 ASEL,S,LOC,X,MX,MX+WV1
 ASEL,R,LOC,Y,MY+(I-1)*WV2,MY+I*WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,MX
 NSEL,R,LOC,Y,MY+(I-1)*WV2,MY+I*WV2
 CEINTF
*ENDDO
ALLS
*DO,I,1,NYC
 ASEL,S,LOC,X,MX+(NXC-1)*WV1,MX+NXC*WV1
 ASEL,R,LOC,Y,MY+(I-1)*WV2,MY+I*WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,MX+NXC*WV1
 NSEL,R,LOC,Y,MY+(I-1)*WV2,MY+I*WV2
 CEINTF
*ENDDO
ALLS

/EOF

PWB_I
C*** Create a PWB Patch for a I-lead component.
C*** This Module produce VOLU=0
C***                AREA=4*(NX+NY)+NXC*NYC+16
C***                LINE=4*area
C***                KP=4*area
*ULIB,data,lib
*USE,arg1     !Lead Info.
*USE,arg2     !Block Info.
*USE,arg3     !solder Info.
```

```
*USE,arg4      !Board Info.
WV0=4*(NX+NY)+NXC*NYC+8
NUM_OFF,4*WV0+32,4*WV0+32,WV0+8,0
WV1=2*(MX+L1-L2P+R1+R2)+NX*(W+SX)-SX
WV2=2*(MY+L1-L2P+R1+R2)+NY*(W+SY)-SY
WV3=L2+L2P+L2M
k,1,-LL,-LH
k,2,2*WV3+WV1+LR,-LH
k,3,2*WV3+WV1+LR,2*WV3+WV2+UH
k,4,-LL,2*WV3+WV2+UH
k,5,0,0
k,6,2*WV3+WV1,0
k,8,0,2*WV3+WV2
k,7,2*WV3+WV1,2*WV3+WV2
!Areas on lower side.
RECT,0,WV3,0,WV3
WPOFF,WV3
RECT,0,MX+L1-L2P+R1+R2,0,WV3
WPOFF,MX+L1-L2P+R1+R2
*DO,I,1,NX-1,1
 RECT,0,W,0,WV3
 WPOFF,W
 RECT,0,SX,0,WV3
 WPOFF,SX
*ENDDO
I=NX
RECT,0,W,0,WV3
WPOFF,W
RECT,0,MX+L1-L2P+R1+R2,0,WV3
WPAVE
!Areas on left side.
WPOFF,,WV3
RECT,0,WV3,0,MY+L1-L2P+R1+R2
WPOFF,,MY+L1-L2P+R1+R2
*DO,I,1,NY-1,1
 RECT,0,WV3,0,W
 WPOFF,,W
 RECT,0,WV3,0,SY
 WPOFF,,Sy
*ENDDO
I=NY
RECT,0,WV3,0,W
WPOFF,,W
RECT,0,WV3,0,MY+L1-L2P+R1+R2
WPAVE
!Line Div. Control.
LSEL,S,LOC,Y,WV3*0.05,WV3*0.95
```

```
LSEL,A,LOC,X,WV3*0.05,WV3*0.95
LESIZE,ALL,,,DL2+DR2,D_RATIO
LSEL,S,LOC,X,WV3*1.05,WV3+(L1+MX-L2P+R1+R2)*0.95
LESIZE,ALL,,,DMX
LSEL,S,LOC,Y,WV3*1.05,WV3+(L1+MY-L2P+R1+R2)*0.95
LESIZE,ALL,,,DMY
*DO,I,1,NX-1,1
 WV4=WV3+MX+L1-L2P+R1+R2+(I-1)*(SX+W)
 LSEL,S,LOC,X,WV4+W*0.05,WV4+W*0.95
 LESIZE,ALL,,,DW
 LSEL,S,LOC,X,WV4+W+SX*0.05,WV4+W+SX*0.95
 LESIZE,ALL,,,DSX
*ENDDO
I=NX
WV4=WV3+MX+L1-L2P+R1+R2+(I-1)*(SX+W)
LSEL,S,LOC,X,WV4+W*0.05,WV4+W*0.95
LESIZE,ALL,,,DW
LSEL,S,LOC,X,WV4+W+(MX+L1-L2P+R1+R2)*0.05,WV4+W+(MX+L1-L2P+R1+R2)*0.95
LESIZE,ALL,,,DMX
*DO,I,1,NY-1,1
 WV4=WV3+MY+L1-L2P+R1+R2+(I-1)*(SY+W)
 LSEL,S,LOC,Y,WV4+W*0.05,WV4+W*0.95
 LESIZE,ALL,,,DW
 LSEL,S,LOC,Y,WV4+W+SY*0.05,WV4+W+SY*0.95
 LESIZE,ALL,,,DSY
*ENDDO
I=NY
WV4=WV3+MY+L1-L2P+R1+R2+(I-1)*(SY+W)
LSEL,S,LOC,Y,WV4+W*0.05,WV4+W*0.95
LESIZE,ALL,,,DW
LSEL,S,LOC,Y,WV4+W+(MY+L1-L2P+R1+R2)*0.05,WV4+W+(MY+L1-L2P+R1+R2)*0.95
LESIZE,ALL,,,DMY
ALLS
!Copy to right and upper side.
ASEL,S,LOC,Y,0,WV3
LOCAL,15,0,XYZ11,XYZ11+WV3+WV2,XYZ11
CSYS,11
ATRAN,15,ALL
ASEL,S,LOC,X,0,WV3
LOCAL,15,0,XYZ11+WV3+WV1,XYZ11,XYZ11
CSYS,11
ATRAN,15,ALL
WPAVE
WV4=WV1/NXC
WV5=WV2/NYC
*DO,I,1,NXC,1
*DO,J,1,NYC,1
```

```
 WPOFF,WV3+(I-1)*WV4,WV3+(J-1)*WV5
 RECT,0,WV4,0,WV5
 WPAVE
*ENDDO
*ENDDO
ASEL,S,LOC,X,WV3,WV3+WV1
ASEL,R,LOC,Y,WV3,WV3+WV2
LSLA
LESIZE,ALL,,,1
a,1,2,6,5
a,2,3,7,6
a,3,4,8,7
a,1,5,8,4
!Generate additional 8 kp, 12 line, 4 area
ASEL,S,LOC,X,-LL,WV3
ASEL,A,LOC,X,WV3+WV1,WV3+WV1+WV3+LR
ASEL,A,LOC,Y,-LH,WV3
ASEL,A,LOC,Y,WV3+WV2,WV3+WV2+WV3+UH
LSLA
LSEL,R,LOC,X,-LL-1,WV3+WV1+WV3+LR+1   ! ANSYS BUG!!!!
ASLL
KSEL,S,KP,,1,4*WV0+8
NUMMRG,KP
AGLUE,ALL
!Create additional 4 areas.
!Line div. for outer lines
LSEL,S,LOC,Y,-LH
LESIZE,ALL,,,DLH
LSEL,S,LOC,Y,WV3+WV2+WV3+UH
LESIZE,ALL,,,DUH
LSEL,S,LOC,X,-LL
LESIZE,ALL,,,DLL
LSEL,S,LOC,X,WV3+WV1+WV3+LR
LESIZE,ALL,,,DLR
LSEL,S,LOC,X,-LL,0
LSEL,R,LOC,Y,-LH,0
LESIZE,ALL,,,D1
LSEL,S,LOC,X,-LL,0
LSEL,R,LOC,Y,WV3+WV2+WV3,WV3+WV2+WV3+UH
LESIZE,ALL,,,D4
LSEL,S,LOC,X,WV3+WV1+WV3,WV3+WV1+WV3+LR
LSEL,R,LOC,Y,-LH,0
LESIZE,ALL,,,D2
LSEL,S,LOC,X,WV3+WV1+WV3,WV3+WV1+WV3+LR
LSEL,R,LOC,Y,WV3+WV2+WV3,WV3+WV2+WV3+UH
LESIZE,ALL,,,D3
ALLS
```

```
MAT,M_NO1
TYPE,1
R,R_NO1,R_V1
REAL,R_NO1
ESHAPE,2  $AMESH,1,WV0
ESHAPE,  $AMESH,WV0+5,WV0+8

*DO,I,1,NXC,1
 ASEL,S,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 ASEL,R,LOC,Y,WV3,WV3+WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,WV3*0.999,WV3*1.001
 NSEL,R,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 CEINTF
*ENDDO
*DO,I,1,NXC,1
 ASEL,S,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 ASEL,R,LOC,Y,WV3+WV2-WV5,WV3+WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,WV3*0.9999+WV2,WV3*1.0001+WV2
 NSEL,R,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 CEINTF
*ENDDO
*DO,I,1,NYC,1
 ASEL,S,LOC,X,WV3,WV3+WV4
 ASEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,WV3*0.999,WV3*1.001
 NSEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 CEINTF
*ENDDO
*DO,I,1,NYC,1
 ASEL,S,LOC,X,WV3+WV1-WV4,WV3+WV1
 ASEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,WV1+WV3*0.999,WV1+WV3*1.001
 NSEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 CEINTF
*ENDDO
```

```
ALLS
/EOF


SOLD_I
C*** Create a solder joint for a I-lead.
C*** This module generate KP=13, Line=15, AREA=7, VOLU=1
C*** arg1 is lead geo. info.<-I_lead0, arg2 is Solder Geo. info.
*ULIB,data,lib
*USE,arg1
*USE,arg2
NUM_OFF,13,15,7,1
k,1,
k,2,L2P+L2+L2M
k,3,L2P+L2,S_H
k,4,L2P,S_H
k,5,L2P-R2,S_H+R2
k,6,L2P,S_H+R2
k,7,L2P+L2+L2M,S_H
k,8,0,S_H+R2
LARC,5,4,6,R2
LARC,3,2,7,(S_H+L2M)*1.1
LARC,1,5,8,(S_H+L2M+R2)*1.1
A,1,2,3,4,5
LESIZE,1,,,DR2
LESIZE,2,,,DS_H
LESIZE,3,,,DS_H
LESIZE,4,,,DR2+DL2,D_RATIO
LESIZE,5,,,DL2
LCCAT,1,5
TYPE,1
MAT,M_NO1
R,R_NO1,R_V1
REAL,R_NO1
ESHAPE,2
AMESH,1
LDEL,6
TYPE,2
MAT,M_NO2
ESIZE,,DW
VEXT,1,,,,,-W
/EOF

J_LEAD
C*** Create a J_lead Model.
C*** Create KP=15, LINE=17, AREA=5, VOLU=0
C*** arg1 = J_LEAD0
```

```
*ULIB,data,lib
*USE,arg1
NUM_OFF,15,17,5,0
K,1,0,R2+H+R1
K,2,L1,R2+H+R1
K,3,L1+R1,R2+H
K,4,L1+R1,R2
K,5,L1+R1-R2
K,6,L1+R1-2*R2,R2
K,7,L1,R2+H
k,8,L1+R1-R2,R2
K,9,0,R2+H+R1,-W
l,1,2
LARC,3,2,7,R1
L,3,4
LARC,5,4,8,R2
LARC,6,5,8,R2
L,1,9

LESIZE,1,,,DL1
LESIZE,2,,,DR1
LESIZE,3,,,DH
LESIZE,4,,,DR2
LESIZE,5,,,DR2
ADRAG,1,2,3,4,5,,6
LSEL,S,LOC,Z,-W*0.1,-W*0.9
LESIZE,ALL,,,DW
ALLS
TYPE,1
MAT,M_NO1
R,R_NO1,R_V1
REAL,R_NO1
AMESH,1,5
LDEL,6
/EOF

SOLD_J
C*** Define a Solder joint connection for a J-LEAD
C*** Create KP=13, LINE=15, AREA=7, VOLU=1
C*** arg1 = J_LEAD0, arg2 = SOLD_J0
*ULIB,data,lib
*USE,arg1
*USE,arg2
NUM_OFF,13,15,7,1
K,1,
K,2,L2P+2*R2+L2M
K,3,L2P+2*R2,S_H+R2
```

```
K,4,L2P+R2,S_H
K,5,L2P,S_H+R2
K,6,L2P+R2,S_H+R2
K,7,L2P+2*R2+L2M,R2+S_H
K,8,,R2+S_H
LARC,5,4,6,R2
LARC,4,3,6,R2
LARC,3,2,7,(R2+S_H+L2M)*1.1
LARC,1,5,8,(R2+S_H+L2M)*1.1
A,1,2,3,4,5
LESIZE,1,,,DR2
LESIZE,2,,,DR2
LESIZE,3,,,DS_H
LESIZE,4,,,DS_H
LESIZE,5,,,2*DR2,D_RATIO
LCCAT,1,2
ALLS
TYPE,1
MAT,M_NO1
R,R_NO1,R_V1
REAL,R_NO1
ESHAPE,2
AMESH,1
LDEL,6
TYPE,2
MAT,M_NO2
ESIZE,,DW
VEXT,1,,,,,-W
ALLS
/EOF


PWB_J
C*** Create a PWB Patch for a J-lead component.
C*** This Module produce VOLU=0
C***                AREA=4*(NX+NY)+NXC*NYC+16
C***                LINE=4*area
C***                KP=4*area
*ULIB,data,lib
*USE,arg1     !Lead Info.
*USE,arg2     !Block Info.
*USE,arg3     !solder Info.
*USE,arg4     !Board Info.
WV0=4*(NX+NY)+NXC*NYC+8
NUM_OFF,4*WV0+32,4*WV0+32,WV0+8,0
L2=2*R2
WV1=2*(MX+L1+R1-L2-L2P)+NX*(W+SX)-SX
```

```
WV2=2*(MY+L1+R1-L2-L2P)+NY*(W+SY)-SY
WV3=L2M+L2+L2P
k,1,-LL,-LH
k,2,2*WV3+WV1+LR,-LH
k,3,2*WV3+WV1+LR,2*WV3+WV2+UH
k,4,-LL,2*WV3+WV2+UH
k,5,0,0
k,6,2*WV3+WV1,0
k,8,0,2*WV3+WV2
k,7,2*WV3+WV1,2*WV3+WV2
!Areas on lower side.
RECT,0,WV3,0,WV3
WPOFF,WV3
RECT,0,MX+(L1+R1-L2)-L2P,0,WV3
WPOFF,MX+(L1+R1-L2)-L2P
*DO,I,1,NX-1,1
 RECT,0,W,0,WV3
 WPOFF,W
 RECT,0,SX,0,WV3
 WPOFF,SX
*ENDDO
I=NX
RECT,0,W,0,WV3
WPOFF,W
RECT,0,MX+(L1+R1-L2)-L2P,0,WV3
WPAVE

!Areas on left side.
WPOFF,,WV3
RECT,0,WV3,0,MY+(L1+R1-L2)-L2P
WPOFF,,MY+(L1+R1-L2)-L2P
*DO,I,1,NY-1,1
  RECT,0,WV3,0,W
 WPOFF,,W
 RECT,0,WV3,0,SY
 WPOFF,,Sy
*ENDDO
I=NY
RECT,0,WV3,0,W
WPOFF,,W
RECT,0,WV3,0,MY+(L1+R1-L2)-L2P
WPAVE
!Line Div. Control
LSEL,S,LOC,Y,WV3*0.05,WV3*0.95
LSEL,A,LOC,X,WV3*0.05,WV3*0.95
LESIZE,ALL,,,2*DR2,D_RATIO
!Lower side
```

```
LSEL,S,LOC,X,WV3*1.0001,WV3+(MX+(L1+R1-L2)-L2P)*0.995
LESIZE,ALL,,,DMX
*DO,I,1,NX-1,1
 WV4=WV3+MX+L1+R1-L2-L2P+(I-1)*(SX+W)
 LSEL,S,LOC,X,WV4+W*0.05,WV4+W*0.95
 LESIZE,ALL,,,DW
 LSEL,S,LOC,X,WV4+W+SX*0.05,WV4+W+SX*0.95
 LESIZE,ALL,,,DSX
*ENDDO
I=NX
WV4=WV3+MX+L1+R1-L2-L2P+(I-1)*(SX+W)
LSEL,S,LOC,X,WV4+W*0.05,WV4+W*0.95
LESIZE,ALL,,,DW
LSEL,S,LOC,X,WV4+W+(MX+L1+R1-L2-L2P)*0.05,WV4+W+(MX+L1+R1-L2-L2P)*0.95
LESIZE,ALL,,,DMX
LSEL,S,LOC,Y,WV3*1.0001,WV3+(MY+(L1+R1-L2)-L2P)*0.995
LESIZE,ALL,,,DMY
*DO,I,1,NY-1,1
 WV4=WV3+MY+L1+R1-L2-L2P+(I-1)*(SY+W)
 LSEL,S,LOC,Y,WV4+W*0.05,WV4+W*0.95
 LESIZE,ALL,,,DW
 LSEL,S,LOC,Y,WV4+W+SY*0.05,WV4+W+SY*0.95
 LESIZE,ALL,,,DSY
*ENDDO
I=NY
WV4=WV3+MY+L1+R1-L2-L2P+(I-1)*(SY+W)
LSEL,S,LOC,Y,WV4+W*0.05,WV4+W*0.95
LESIZE,ALL,,,DW
LSEL,S,LOC,Y,WV4+W+(MY+L1+R1-L2-L2P)*0.05,WV4+W+(MY+L1+R1-L2-L2P)*0.95
LESIZE,ALL,,,DMY
!Copy lower and left side to upper and right side
ASEL,S,LOC,Y,0,WV3
LOCAL,15,0,XYZ11,XYZ11+WV3+WV2,XYZ11
CSYS,11
ATRAN,15,ALL
ASEL,S,LOC,X,0,WV3
LOCAL,15,0,XYZ11+WV3+WV1,XYZ11,XYZ11
CSYS,11
ATRAN,15,ALL

WPAVE
WV4=WV1/NXC
WV5=WV2/NYC
*DO,I,1,NXC,1
*DO,J,1,NYC,1
 WPOFF,WV3+(I-1)*WV4,WV3+(J-1)*WV5
 RECT,0,WV4,0,WV5
```

```
 WPAVE
*ENDDO
*ENDDO
ASEL,S,LOC,X,WV3,WV3+WV1
ASEL,R,LOC,Y,WV3,WV3+WV2
LSLA
LESIZE,ALL,,,1
a,1,2,6,5
a,2,3,7,6
a,3,4,8,7
a,1,5,8,4
!Generate additional 8 kp, 12 line, 4 area
ASEL,S,LOC,X,-LL,WV3
ASEL,A,LOC,X,WV3+WV1,WV3+WV1+WV3+LR
ASEL,A,LOC,Y,-LH,WV3
ASEL,A,LOC,Y,WV3+WV2,WV3+WV2+WV3+UH
LSLA
LSEL,R,LOC,X,-LL-1,WV3+WV1+WV3+LR+1   !ANSYS BUGS
ASLL
KSLL
NUMMRG,KP
AGLUE,ALL
!Create additional 4 areas.
LSEL,S,LOC,Y,-LH
LESIZE,ALL,,,DLH
LSEL,S,LOC,Y,WV3+WV2+WV3+UH
LESIZE,ALL,,,DUH
LSEL,S,LOC,X,-LL
LESIZE,ALL,,,DLL
LSEL,S,LOC,X,WV3+WV1+WV3+LR
LESIZE,ALL,,,DLR
LSEL,S,LOC,X,-LL,0
LSEL,R,LOC,Y,-LH,0
LESIZE,ALL,,,D1
LSEL,S,LOC,X,-LL,0
LSEL,R,LOC,Y,WV3+WV2+WV3,WV3+WV2+WV3+UH
LESIZE,ALL,,,D4
LSEL,S,LOC,X,WV3+WV1+WV3,WV3+WV1+WV3+LR
LSEL,R,LOC,Y,-LH,0
LESIZE,ALL,,,D2
LSEL,S,LOC,X,WV3+WV1+WV3,WV3+WV1+WV3+LR
LSEL,R,LOC,Y,WV3+WV2+WV3,WV3+WV2+WV3+UH
LESIZE,ALL,,,D3
ALLS
MAT,M_NO1
TYPE,1
R,R_NO1,R_V1
```

```
REAL,R_NO1
ESHAPE,2   $AMESH,1,WV0
ESHAPE,   $AMESH,WV0+5,WV0+8
*DO,I,1,NXC,1
 ASEL,S,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 ASEL,R,LOC,Y,WV3,WV3+WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,WV3*0.999,WV3*1.001
 NSEL,R,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 CEINTF
*ENDDO
*DO,I,1,NXC,1
 ASEL,S,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 ASEL,R,LOC,Y,WV3+WV2-WV5,WV3+WV2
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,Y,WV3*0.9999+WV2,WV3*1.0001+WV2
 NSEL,R,LOC,X,WV3+(I-1)*WV4,WV3+I*WV4
 CEINTF
*ENDDO
*DO,I,1,NYC,1
 ASEL,S,LOC,X,WV3,WV3+WV4
 ASEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,WV3*0.999,WV3*1.001
 NSEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 CEINTF
*ENDDO
*DO,I,1,NYC,1
 ASEL,S,LOC,X,WV3+WV1-WV4,WV3+WV1
 ASEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 ESLA
 NSLE
 NSEL,INVE
 NSEL,R,LOC,X,WV1+WV3*0.999,WV1+WV3*1.001
 NSEL,R,LOC,Y,WV3+(I-1)*WV5,WV3+I*WV5
 CEINTF
*ENDDO
ALLS
/EOF
```

```
FCOB
C*** Create a Flip-Chip with Board.
C*** Generate KP=80, Line=120, AREA=60, VOLU=12
*ULIB,data,lib
*USE,arg1
NUM_OFF,80,100,60,12
K,1,L1/2,-L2/2
K,2,L1/2+F_L,-L2/2
K,3,L1/2,-L2/2,H1
K,4,L1/2,-L2/2,H1+H2
K,5,L1/2+F_L,-L2/2,H1+H2
LARC,4,2,5,R
A,1,2,4,3
LESIZE,1,,,DR,-2
LESIZE,2,,,DF_L
LESIZE,3,,,DH2
LESIZE,4,,,DH1
MAT,M_NO1
TYPE,1
R,R_NO1,R_V1
REAL,R_NO1
AMESH,1
MAT,M_NO2  $ TYPE,2
ESIZE,,DRO
VROT,1,,,,,,4,1,90
ESIZE,,DL2
VEXT,1,,,,L2
MAT,M_NO1  $TYPE,1  $REAL,R_NO1
AMESH,4
MAT,M_NO2  $TYPE,2
ESIZE,,DL1
VEXT,4,,,-L1
LOCAL,15,0,XYZ11,XYZ11,XYZ11,180
CSYS,11
VTRAN,15,1,3
LOCAL,14,0,XYZ11+L1/2,XYZ11-L2/2,XYZ11
LOCAL,15,0,XYZ11+L1/2,XYZ11+L2/2,XYZ11,90
CSYS,14
VTRAN,15,1
LOCAL,15,0,XYZ11-L1/2,XYZ11-L2/2,XYZ11,270
CSYS,14
VTRAN,15,1
CSYS,11
BLOCK,-L1/2,L1/2,-L2/2,L2/2,0,H1
BLOCK,-L1/2,L1/2,-L2/2,L2/2,H1,H1+H2
VSEL,S,VOLU,,9,10
ASLV
```

```
LSLA
LSEL,R,LOC,Z,0+H1*0.1,H1*0.9
LESIZE,ALL,,,DH1
LSLA
LSEL,R,LOC,Z,H1+H2*0.1,H1+H2*0.9
LESIZE,ALL,,,DH2
LSLA
LSEL,R,LOC,X,-L1/2*0.9,L1/2*0.9
LESIZE,ALL,,,DL1
LSLA
LSEL,R,LOC,Y,-L2/2*0.1,L2/2*0.1
LESIZE,ALL,,,DL2
MAT,M_NO3 $TYPE,2  $VMESH,10
MAT,M_NO2 $TYPE,2  $VMESH,9
RECT,-L1/2-F_L-LL,L1/2+F_L+LR,-L2/2-F_L-LH,UH+L2/2+F_L
asel,s,loc,z,0
aovlap,all
NSEL,S,LOC,Z,0,(H1+H2)*1.0001
ESLN
NUMMRG,NODE
KSEL,S,LOC,Z,0,(H1+H2)*1.0001
NUMMRG,KP
LSEL,S,LOC,X,(-L1/2-F_L-LL)*1.001,(-L1/2-F_L-LL)*0.999
LESIZE,ALL,,,DLL
LSEL,S,LOC,X,(L1/2+F_L+LR)*0.999,(L1/2+F_L+LR)*1.001
LESIZE,ALL,,,DLR
LSEL,S,LOC,Y,(-F_L-L2/2-LH)*1.001,(-F_L-L2/2-LH)*0.999
LESIZE,ALL,,,DLH
LSEL,S,LOC,Y,(UH+L2/2+F_L)*0.999,(UH+L2/2+F_L)*1.001
LESIZE,ALL,,,DUH
ASLL
MAT,M_NO4  $TYPE,1
R,R_NO4,R_V4  $REAL,R_NO4
AMESH,ALL
VSEL,S,LOC,Z,0,H1+H2
ASLV
ASEL,R,LOC,Z,0
AMESH,ALL
AGEN,2,ALL,,,,0
VSEL,S,LOC,Z,0,H1+H2
ASLV
ASEL,R,LOC,Z,0
ACLEAR,ALL
ALLS
/EOF
```

Part 3. Sample Data Input File:

```
BLOCK1
C*** For a TSOP with 4 side Leads.
C*** Define a Plastic Block for a I or J Lead TSOP
C*** REAL 11 is the thickness of block.
LEADSIDE=4
W=12  $DW=2
MX=18   $DMX=2
MY=18   $DMY=2
NX=10
NY=10
NXC=7
NYC=7
SX=12   $DSX=1
SY=12   $DSY=1
M_NO1=PLAS1  $R_NO1=11   $R_V1=21
/EOF

I_LEAD1
C*** Define the geometry of a Gull-Lead -> I-lead.
L1=8      $DL1=2
L2=8      $DL2=3
 H=15      $ DH=2
R1=5   $DR1=3
R2=5     $DR2=3
W=12       $DW=2
T=1
M_NO1=LEAD1 $R_NO1=12  $R_V1=T  !R_NO1 here is unique.
                    !Start from 11 for nonglobal R type definition.
/EOF

PWB_I1
C*** Define a Board Geo. corresponding to a I-lead Component.
C*** PWB_I0 OVERWRITE BLOCK0 DATA.
X0=0  $Y0=380   $Z0=0   $ROT0=0
LL=40   $LR=40   $LH=38   $UH=38
DLL=38  $DLR=50  $DLH=45 $DUH=36
D1=7    $D2=7    $D3=7   $D4=7
DMX=3   $DMY=3   $DSX=1   $DSY=1
!DMX=MX+L1=L2P, These Par. are for PWB board patch.
NXC=9   $NYC=9  !Overwrite the NXC and NYC in BLOCK.
M_NO1=PWB    $R_NO1=PWB_R    $R_V1=PWB_T
/EOF

SOLD_I1
C*** Solder joint Geometry for I-lead.

L2P=R2+3  $L2M=4 !Solder joint extension above a Lead.
```

```
S_H=2.5 !Solder joint height of coplanarity.
DS_H=3
D_ratio=-2
M_NO1=TRASH    $R_NO1=TRASH_R    $R_V1=TRASH_T
M_NO2=SOLDER
/EOF


FCOB1
C*** Define a DCA geo. and final location.
C*** DCA include Die ENCAP and Fr4 board.
X0=0   $Y0=0  $Z0=0   $ROT0=0
L1=150  $L2=150
DL1=10  $DL2=10
H1=5    $H2=25
DH1=2   $DH2=3
F_L=35  $R=50
DF_L=4  $DR=7 $DRO=4
B_L1=20 $B_L2=30
LL=92  $LH=80   $LR=92   $UH=80
DLL=26 $DLH=26  $DLR=36  $DUH=45
M_NO1=TRASH  $R_NO1=TRASH_R  $R_V1=TRASH_T
M_NO2=EPOXY
M_NO3=SILICON
M_NO4=PWB    $R_NO4=PWB_R    $R_V4=PWB_T
/EOF

BLOCK2
C*** For a TSOP with 4 side Leads.
C*** Define a Plastic Block for a I or J Lead TSOP
C*** REAL 11 is the thickness of block.
LEADSIDE=4
W=12  $DW=2
MX=20   $DMX=2
MY=20   $DMY=2
NX=8
NY=8
NXC=6
NYC=6
SX=13   $DSX=1
SY=13   $DSY=1
M_NO1=PLAS1  $R_NO1=13   $R_V1=21
/EOF

J_LEAD2
C*** Define geometry of a J-lead.
W=12   $DW=2
```

```
L1=6  $DL1=2
R1=4  $DR1=3
H=8   $DH=3
R2=5 $DR2=3   !DR2*2= Total div. of lower J-lead div.
M_NO1=LEAD1  $R_NO1=14  $R_V1=0.5  !R_No1=12 is local deinfed
                        !It should be unique!!!
/EOF

SOLD_J2
C*** Define a Solder joint connection for a J-LEAD.
L2P=3.
L2M=4.
S_H=2.5. !Solder joint height of coplanarity.
DS_H=3
D_ratio=-2
M_NO1=TRASH    $R_NO1=TRASH_R    $R_V1=TRASH_T
M_NO2=SOLDER
/EOF

PWB_J2
C*** Define a Board Geo. corresponding to a I-lead Component.
C*** PWB_I0 OVERWRITE BLOCK0 DATA.
X0=404  $Y0=0   $Z0=0   $ROT0=0
LL=52   $LR=53   $LH=62   $UH=63
DLL=36  $DLR=44  $DLH=36 $DUH=40
D1=7    $D2=7    $D3=7   $D4=7
DMX=3   $DMY=3   $DSX=1   $DSY=1
!DMX=MX+L1=L2P, These Par. are for PWB board patch.
NXC=8   $NYC=8  !Overwrite the NXC and NYC in BLOCK.
M_NO1=PWB    $R_NO1=PWB_R    $R_V1=PWB_T
/EOF

RE2_1
C***
X0=404  $Y0=380+160  $Z0=0  $ROT0=0
H1=2  $H2=12
DH1=2 $DH2=4
L1=4  $L2=12  $L3=20
DL1=2 $DL2=DH1+DH2 $DL3=4
W=12   $R=20
DW=3
LL=54  $LH=34  $LR=54  $UH=34
DLL=15 $DLH=10 $DLR=15 $DUH=10
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
```

```
/EOF

RE2_2
C***
X0=404+120  $Y0=380+160  $Z0=0  $ROT0=0
H1=2  $H2=12
DH1=2 $DH2=4
L1=4  $L2=12  $L3=20
DL1=2 $DL2=DH1+DH2 $DL3=4

W=12   $R=20
DW=3

LL=54  $LH=34  $LR=54  $UH=34
DLL=15 $DLH=10 $DLR=15 $DUH=12
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/EOF


RE2_3
C***
X0=404+240  $Y0=380+160  $Z0=0  $ROT0=0
H1=3  $H2=22
DH1=2 $DH2=4
L1=8  $L2=16  $L3=34
DL1=2 $DL2=DH1+DH2 $DL3=4
W=20   $R=45
DW=3
LL=50  $LH=19  $LR=50  $UH=19
DLL=15 $DLH=10 $DLR=12 $DUH=12
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/EOF

RE2_4
C***
X0=404  $Y0=380+400  $Z0=0  $ROT0=-90
H1=3  $H2=22
DH1=2 $DH2=4
L1=8  $L2=16  $L3=34
DL1=2 $DL2=DH1+DH2 $DL3=4
W=20   $R=45
```

```
DW=3
LL=50  $LH=19  $LR=50  $UH=19
DLL=10 $DLH=15 $DLR=10 $DUH=15
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/EOF

RE2_5
C***
X0=404+120  $Y0=380+400  $Z0=0  $ROT0=-90
H1=2  $H2=12
DH1=2 $DH2=4
L1=4  $L2=12  $L3=20
DL1=2 $DL2=DH1+DH2 $DL3=4
W=12   $R=20
DW=3

LL=54  $LH=34  $LR=54  $UH=34
DLL=10 $DLH=15 $DLR=12 $DUH=15
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/EOF


RE2_6
C***
X0=404+240  $Y0=380+400  $Z0=0  $ROT0=-90
H1=2  $H2=12
DH1=2 $DH2=4
L1=4  $L2=12  $L3=20
DL1=2 $DL2=DH1+DH2 $DL3=4
W=12   $R=20
DW=3
LL=54  $LH=34  $LR=54  $UH=34
DLL=10 $DLH=15 $DLR=12 $DUH=12
D1=8  $D2=8  $D3=8  $D4=8
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/EOF

RE3_1
C*** Define the a Resistor with 3 Leads.
```

```
C*** One on left side, two on right side.
C*** Rotate the direction for different application.
C*** THese should be global variables.
C*** TRASH,TRASH_R, TRASH_T, SOLDER, PLAS1,PWB, PWB_T,PWB_R
 ! Define the final location of the Re. Component.
 X0=404  $Y0=380  $Z0=0  $ROT0=0
H1=4  $H2=10  $H3=10          !H1->Re'height to PWB, h2-> solder height on Re.
                    !H3->Re's height above solder.
DH1=2 $DH2=4 $DH3=2         !DH1+DH2-> has to be EVEN Number.
L1=30/2  $L2=20              !L1->re's width/2 L2-> solder base length .
DL1=4 $DL2=DH1+DH2
MY=14  $W=15  $SY=18          !MY->Lead y-mrgine to lower side
                    !W ->solder joint width, SY-> y-seperation.
DMY=2 $DW=2 $DSY=1
R=35
DR=DL2
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
! For PWB associated with this Re.
LL=55  $LH=56  $LR=55  $UH=56
DLL=20 $DLH=20 $DLR=15 $DUH=15
D_1=8 $D_2=8 $D_3=8 $D_4=8
DL11=4 ! Center line div. for PWB of Re.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/eof

RE3_2
C*** Define the a Resistor with 3 Leads.
C*** One on left side, two on right side.
C*** Rotate the direction for different application.
C*** THese should be global variables.
C*** TRASH,TRASH_R, TRASH_T, SOLDER, PLAS1,PWB, PWB_T,PWB_R
 ! Define the final location of the Re. Component.
 X0=404+180  $Y0=380+160  $Z0=0  $ROT0=-90
H1=4  $H2=10  $H3=10          !H1->Re'height to PWB, h2-> solder height on Re.
                    !H3->Re's height above solder.
DH1=2 $DH2=4 $DH3=2         !DH1+DH2-> has to be EVEN Number.
L1=30/2  $L2=20              !L1->re's width/2 L2-> solder base length .
DL1=4 $DL2=DH1+DH2
MY=14  $W=15  $SY=18          !MY->Lead y-mrgine to lower side
                    !W ->solder joint width, SY-> y-seperation.
DMY=2 $DW=2 $DSY=1
R=35
DR=DL2
M_NO1=TRASH  $R_NO1=TRASH_R $R_V1=TRASH_T ! for volume ext.
M_NO2=SOLDER $M_NO3=PLAS1 ! for solder joint and body plastic.
! For PWB associated with this Re.
```

```
LL=45  $LH=66  $LR=45  $UH=66
DLL=15 $DLH=15 $DLR=20 $DUH=16
D_1=8 $D_2=8 $D_3=8 $D_4=8
DL11=4 ! Center line div. for PWB of Re.
M_NO4=PWB  $R_NO4=PWB_R  $R_V4=PWB_T  ! for fr4 PWB
/eof


BLOCK3
C*** For a TSOP with 4 side Leads.
C*** Define a Plastic Block for a I or J Lead TSOP
C*** REAL 11 is the thickness of block.
LEADSIDE=2
W=12  $DW=2
MX=18   $DMX=2
MY=18   $DMY=2
NX=6
NY=8
NXC=5
NYC=8
SX=12   $DSX=1
SY=15   $DSY=1
M_NO1=PLAS1  $R_NO1=11   $R_V1=21
/EOF

I_LEAD3
C*** Define the geometry of a Gull-Lead -> I-lead.
L1=8      $DL1=2
L2=8      $DL2=3
 H=15      $ DH=2
R1=5   $DR1=3
R2=5     $DR2=3
W=12       $DW=2
T=1
M_NO1=LEAD1 $R_NO1=12  $R_V1=T  !R_NO1 here is unique.
                        !Start from 11 for nonglobal R type definition.
/EOF

PWB_I3
C*** Define a Board Geo. corresponding to a I-lead Component.
C*** PWB_I0 OVERWRITE BLOCK0 DATA.
X0=404+360  $Y0=380   $Z0=0   $ROT0=-90
!LL=86   $LR=86   $LH=43   $UH=40
!DLL=44  $DLR=38  $DLH=45 $DUH=48
LL=76   $LR=76   $LH=53   $UH=50
DLL=48  $DLR=45  $DLH=44 $DUH=38
D1=9    $D2=9    $D3=9   $D4=9
```

```
DMX=3   $DMY=3   $DSX=1   $DSY=1
!DMX=MX+L1=L2P, These Par. are for PWB board patch.
NXC=6   $NYC=8  !Overwrite the NXC and NYC in BLOCK.
M_NO1=PWB    $R_NO1=PWB_R    $R_V1=PWB_T

/EOF

SOLD_I3
C*** Solder joint Geometry for I-lead.
L2P=R2+3  $L2M=4 !Solder joint extension above a Lead.
S_H=2.5 !Solder joint height of coplanarity.
DS_H=3
D_ratio=-1.5
M_NO1=TRASH    $R_NO1=TRASH_R    $R_V1=TRASH_T
M_NO2=SOLDER
/EOF

FCOB2
C*** Define a DCA geo. and final location.
C*** DCA include Die ENCAP and Fr4 board.
X0=764   $Y0=380+400  $Z0=0   $ROT0=-90
L1=220  $L2=140
DL1=14  $DL2=10
H1=5    $H2=33
DH1=2   $DH2=4
F_L=40  $R=50
DF_L=4  $DR=7 $DRO=4
B_L1=20 $B_L2=30
!LL=50  $LH=90   $LR=50   $UH=90
!DLL=40 $DLH=48  $DLR=30  $DUH=30
LL=50  $LH=90   $LR=50   $UH=90
DLL=30 $DLH=40  $DLR=48  $DUH=30
M_NO1=TRASH  $R_NO1=TRASH_R  $R_V1=TRASH_T
M_NO2=EPOXY
M_NO3=SILICON
M_NO4=PWB    $R_NO4=PWB_R    $R_V4=PWB_T
/EOF
```